HUAWEI 30 mm × 30 mm LGA Module

Hardware Migration Guide

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About This Document

Revision History

Document Version	Date	Chapter	Descriptions
01	2011-05-17		Creation
02	2013-10-11	All	Updated
03	2014-02-18	All	Updated the description related to LED pins
			Updated the description related to UART pins
			Updated the description related to PCM audio pins
		3.5	Updated antenna interface compatibility design
04	2014-10-11	All	Added the description related to MU709 and ME909u-523
05	2015-03-17	All	Added the description related to ME209u-526
06	2015-10-27	All	Added the description related to ME909s
07	2016-04-08	All	Added the description related to MU509-65
		3.2.1	Deleted Table 3-2 Differences of the antenna interface in pad size and function
		3.3.2	Updated stencil thickness from 0.15 mm to 0.12 mm
08	2016-12-12	1	Updated Table 1-2 Overview of Huawei 30 mm × 30 mm LGA modules and Table 1-3 Differences of LGA Interfaces
		2.3.1	Deleted the description related to MU609
		2.3.1	Updated Table 2-9 Differences of the audio interface

Document Version	Date	Chapter	Descriptions
		2.3.2	Deleted the description related to MU609
		2.3.2	Updated Figure 2-11 The recommended connection of the PCM interface in the LGA module
		2.3.3	Deleted the description related to MU609
		4	Updated Table 4-1 Definition of LGA Interfaces

Contents

1 Overview

This document describes interface differences among Huawei Land Grid Array (LGA) series modules of 30 mm × 30 mm (size). With this document, you can learn interface differences among the MU509 (including MU509-b, MU509-c, MU509-65 and MU509-g), MC509 (including MC509 and MC509-a), MU609, ME209u-526, ME909u (including ME909u-521 and ME909u-523), MU709 (including MU709s-2 and MU709s-6), and ME909s (including ME909s-821 and ME909s-120) and precautions for compatibility design of the preceding modules.

Table 1-1 Bands and Rates of Huawei 30 mm × 30 mm LGA modules

Product	Bands	Rates
MU509-b	WCDMA Band 1/8 GSM/GPRS/EDGE: 1900 MHz/1800 MHz/900 MHz/850 MHz	GSM CS: UL 14.4 kbit/s; DL 14.4 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSDPA: DL 3.6 Mbit/s
MU509-c	WCDMA Band 2/5 GSM/GPRS/EDGE: 1900 MHz/1800 MHz/900 MHz/850 MHz	GSM CS: UL 14.4 kbit/s; DL 14.4 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSDPA: DL 3.6 Mbit/s
MU509-65	WCDMA Band 2/5	WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSDPA: DL 3.6 Mbit/s

Product	Bands	Rates
MU509-g	WCDMA Band 1/5 GSM/GPRS/EDGE: 1900 MHz/1800 MHz/900 MHz/850 MHz	GSM CS: UL 14.4 kbit/s; DL 14.4 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSDPA: DL 3.6 Mbit/s
MC509	CDMA BC 0/1 GPS Standalone	CDMA 1xRTT: UL 153.6 kbit/s; DL 153.6 kbit/s CDMA 1x EVDO Rev.A: UL 1.8 Mbit/s; DL 3.1 Mbit/s
MC509-a	CDMA BC 0 GPS Standalone	CDMA 1xRTT: UL 153.6 kbit/s; DL 153.6 kbit/s CDMA 1x EVDO Rev.A: UL 1.8 Mbit/s; DL 3.1 Mbit/s
MU609	WCDMA Band 1/2/5/8 GSM/GPRS/EDGE: 850 MHz/900 MHz/1800 MHz/1900 MHz GPS Standalone/A-GPS	GSM CS: UL 14.4 kbit/s; DL 14.4 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSDPA: UL 5.76 Mbit/s; DL 14.4 Mbit/s
ME209u-526	LTE Band 4/13	LTE FDD: UL 50 Mbit/s; @20M BW cat3; DL 100 Mbit/s
ME909u-521	LTE Band 1/2/3/5/7/8/20 WCDMA Band1/2/5/8 GSM/GPRS/EDGE: 1900 MHz/1800 MHz/900 MHz/850 MHz GPS Standalone/A-GPS	LTE FDD: UL 50 Mbit/s @20M BW cat3; DL 100 Mbit/s DC-HSPA+: UL 5.76 Mbit/s; DL 43.2 Mbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s
ME909u-523	LTE Band 2/4/5/17 WCDMA Band 2/4/5 GPS Standalone/A-GPS	LTE FDD: UL 50 Mbit/s; @20M BW cat3; DL 100 Mbit/s DC-HSPA+: UL 5.76 Mbit/s; DL 43.2 Mbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s; WCDMA PS: UL 384 kbit/s; DL 384 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s

Product	Bands	Rates
MU709s-6	WCDMA Band 1/2/5 GSM/GPRS/EDGE: 850 MHz/900 MHz/1800 MHz/1900 MHz	GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s
MU709s-2	WCDMA Band 1/8 GSM/GPRS/EDGE: 850 MHz/900 MHz/1800 MHz/1900 MHz	GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s
ME909s-821	FDD LTE: Band 1, Band 3, Band 8, all bands with diversity TDD LTE: Band 38, Band 39, Band 40, Band 41, all bands with diversity DC-HSPA+/HSPA+/HSPA/WCDMA: Band 1, Band 5, Band 8, Band 9, all bands with diversity TD-SCDMA: Band 34, Band 39 GSM/GPRS/EDGE: 1800 MHz/900 MHz	GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s DC-HSPA+: UL 5.76 Mbit/s; DL 42 Mbit/s TD-HSPA: UL 2.2 Mbit/s; DL 2.8 Mbit/s TD-SCDMA PS: UL 384 kbit/s; DL 2.8 Mbit/s LTE FDD: UL 50 Mbit/s; DL 150 Mbit/s @20M BW cat4 LTE TDD: UL 10 Mbit/s; DL 112 Mbit/s @20M BW cat4 (Uplink-downlink configuration 2, 1:3)
ME909s-120	FDD LTE: Band 1, Band 2, Band 3, Band 4, Band 5, Band 7, Band 8, Band 20, all bands with diversity WCDMA/HSDPA/HSUPA/HSPA+: Band 1, Band 2, Band 5, Band 8, all bands with diversity GSM/GPRS/EDGE: 850 MHz/900 MHz/1800 MHz/1900 MHz	GPRS: UL 85.6 kbit/s; DL 85.6 kbit/s EDGE: UL 236.8 kbit/s; DL 236.8 kbit/s WCDMA CS: UL 64 kbit/s; DL 64 kbit/s WCDMA PS: UL 384 kbit/s; DL 384 kbit/s HSPA+: UL 5.76 Mbit/s; DL 21.6 Mbit/s DC-HSPA+: UL 5.76 Mbit/s; DL 42 Mbit/s LTE FDD: UL 50 Mbit/s; DL 150 Mbit/s @20M BW cat4

Table 1-2 Overview of Huawei 30 mm × 30 mm LGA modules

Product	Interface	Temperature	Dimension (mm)
MU509	1 x USIM 1 × 8 wire UART 1 × USB (Full Speed) 2 × Microphone in 1 × Handset out 1 × Speaker out 1 × PCM 8 × GPIO 2 × LED 1 × JTAG 1 ×WAKEUP_IN 1 ×WAKEUP_OUT 1 × Antenna	Normal operating temperature: –20°C to +70°C Extended operating temperature: –40°C to +85°C Storage Temperature: –40°C to +85°C **Only for MU509-65: Normal operating temperature: –30°C to +75°C**	30 × 30 × 2.6
MC509	1 x UIM 1 × 8 wire UART 1 × USB (Full Speed) 2 × Microphone in 1 × Handset out 1 × Speaker out 1 × PCM 7 × GPIO 2 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × W_DISABLE 3 × Antenna	Normal operating temperature: –20°C to +70°C Extended operating temperature: –30°C to +75°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.65
MU609	1 x USIM 1 × 8 wire UART 1 × 2 wire UART (Debug) 1 × USB (High Speed) 5 × GPIO 1 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × SLEEP_STATUS 3 × Antenna	Normal operating temperature: –20°C to +70°C Extended operating temperature: –40°C to +85°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.27

Product	Interface	Temperature	Dimension (mm)
ME209u-526	1 x USIM 2 × 4 wire UART 1 × 2 wire UART (Debug) 1 × USB (High Speed) 1 × PCM[1] 5 × GPIO 2 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × SLEEP_STATUS 2× Antenna 2 x ADC	Normal operating temperature: –30°C to +75°C Extended operating temperature: –40°C to +85°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.35
ME909u	1 x USIM 2 × 4 wire UART 1 × 2 wire UART (Debug) 1 × USB (High Speed) 1 × PCM[2] 5 × GPIO 2 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × SLEEP_STATUS 3 × Antenna **2 x ADC is only for ME909u-523**	Normal operating temperature: –20°C to +70°C Extended operating temperature: –30°C to +75°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.35

Product	Interface	Temperature	Dimension (mm)
MU709	1 x USIM 1 x USIM_DET 1 × 8 wire UART 1 × 2 wire UART (Debug) 1 × USB (High Speed) 1 × PCM 5 × GPIO 1 × LED 1 × JTAG 1 × Wakeup_In 1 × Wakeup_Out 1 × SLEEP_STATUS 2 × Antenna	Normal operating temperature: –20°C to +70°C Extended operating temperature: –40°C to +85°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.27
ME909s-821	1 x USIM 1 x USIM_DET 1 × 8 wire UART 1 × 2 wire UART (Debug) 1 × USB (High Speed) 1 × PCM 7 × GPIO 1 × LED 1 × JTAG 1 ×WAKEUP_IN 1 ×WAKEUP_OUT 1 × SLEEP_STATUS 2 × Antenna 2 x ADC	Normal operating temperature: –30°C to +75°C Extended operating temperature: –40°C to +85°C Storage Temperature: –40°C to +85°C	30 × 30 × 2.57
ME909s-120			30 × 30 × 2.52

NOTE

- [1]: The firmware of ME209u-526 does not support PCM function yet.
- [2]: The firmware of ME909u-521 supports PCM function and the firmware of ME909u-523 does not support PCM function.

Figure 1-2 Huawei 30 mm × 30 mm LGA module block level functional compatibility

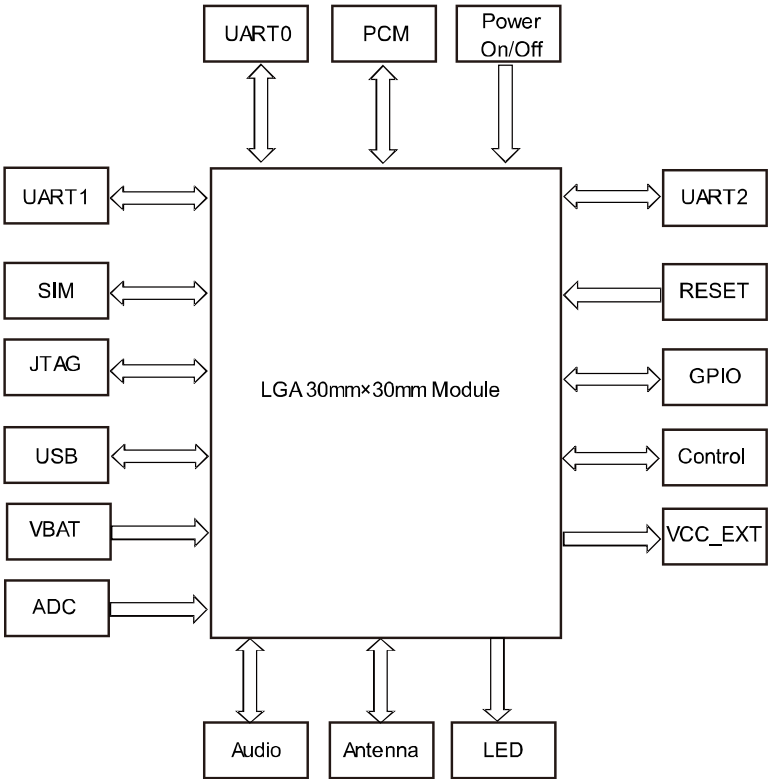


Table 1-3 Differences of LGA Interfaces

Pin No.	Interface	Description	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
11	Control	WAKEUP_IN	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
71		WAKEUP_OUT	CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
45		W_DISABLE	GPIO CMOS 2.6 V	CMOS 2.6 V	Reserved	Reserved	Reserved	Reserved	Reserved
15		SLEEP_STATUS	Reserved	Reserved	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
70		USIM_DET	N	N	N	N	N	Y	Y
81		POWER_ON_OFF	Y	Y	Y	Y	Y	Y	Y
100		RESIN_N	Y	Y	Y	Y	Y	Y	Y
5–8	Audio	PCM audio	CMOS 2.6 V	CMOS 2.6 V	N	CMOS 1.8 V[1]	CMOS 1.8 V[1] [2]	CMOS 1.8 V	CMOS 1.8 V
38–41 and 96–99		Analog audio	Y	Y	N	N	N	N	N
43	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO
44	GPIO	GPIO	CMOS 2.6 V	CMOS 2.6 V	Reserved	Reserved	Reserved	Reserved	Reserved
46			CMOS 2.6 V	CMOS 2.6 V	Reserved	Reserved	Reserved	Reserved	GPIO
51, 55, 105, 109 and 113			CMOS 2.6 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
107 and 111, 115	Antenna	ANT pad size	1.5 mm × 1.0 mm	1.5 mm × 1.0 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm	1.02 mm × 0.82 mm

Pin No.	Interface	Description	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
107, 111 and 115		ANT function	Main (pin 107)	Main (pin 107), AUX (pin 115), GPS (pin 111)	Main (pin 107), AUX (pin 115), GPS (pin 111)	Main (pin 107), AUX (pin 115)	Main (pin 107), AUX (pin 115), GPS (pin 111)	Main (pin 107), AUX (pin 115)	Main (pin 107), AUX (pin 115)
31	VCC_EXT	VCC_EXT2 (2.6 V)	Y	Y	N	N	N	N	N
32		VCC_EXT1 (1.8 V)	Y	Y	Y	Y	Y	Y	Y
12 and 13	VBAT[4]	VBAT (3.3 V–4.2 V) VBAT (3.2 V–4.2 V) is only for ME909s	Five 220 µF capacitors needed	A 220 µF capacitor needed	Five 220 µF capacitors needed	Five 220 µF capacitors needed	Five 220 µF capacitors needed	Five 220 µF capacitors needed	Five 220 µF capacitors needed
30, 36, 42, 47, 72, 87 and 93	JTAG	JTAG	CMOS 1.8 V	CMOS 2.6 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V
14		PS_HOLD	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	CMOS 1.8 V	N
100/47		RESIN_N/JTAG_SRST_N	RESIN_N (pin 100)	RESIN_N (pin 100)	RESIN_N (pin 100)	**JTAG_SRST_N (pin 47)** **JTAG reset for debugging**	**JTAG_SRST_N (pin 47)** **JTAG reset for debugging**	RESIN_N (pin 100)	RESIN_N (pin 100)
73–80	UART	UART0	8-wire UART CMOS 2.6 V	8-wire UART CMOS 2.6 V	8-wire UART CMOS 1.8 V	4-wire UART CMOS 1.8V	4-wire UART CMOS 1.8V	8-wire UART CMOS 1.8 V	8-wire UART CMOS 1.8 V
1–4		UART1	N	N	2-wire UART CMOS 1.8 V for debugging	4-wire UART CMOS 1.8V	4-wire UART CMOS 1.8V	2-wire UART CMOS 1.8 V for debugging	N

Pin No.	Interface	Description	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
28 and 29		UART2	Reserved	Reserved	N	2-wire UART CMOS 1.8 V only for debugging.	2-wire UART CMOS 1.8 V only for debugging.	N	2-wire UART CMOS 1.8 V only for debugging .
85 and 86	USB	USB protocol	USB 2.0 Full Speed	USB 2.0 Full Speed	USB 2.0 High Speed	USB 2.0 High Speed	USB 2.0 High Speed	USB 2.0 High Speed	USB 2.0 High Speed
91	LED	LED_STATUS	Y	Y	N	N	N	N	N
101		LED_MODE	Y	Y	Y	Y	Y	Y	Y
34	SIM/USIM /RUIM	USIM_VCC/RUIM_ VCC	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/3.0 V	1.8 V/3.0 V
88		USIM_RESET/RUI M_RESET	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/3.0 V	1.8 V/3.0 V
89		USIM_DATA/RUIM _DATA	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/3.0 V	1.8 V/3.0 V
90		USIM_CLK/RUIM_ CLK	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/2.85 V	1.8 V/3.0 V	1.8 V/3.0 V
102 and 104	ADC	ADC	N	N	N	Y 0.3 V–VBAT	Y[3] 0.3 V–VBAT	N	Y 0 V–2.5 V
49, 53 and 57	GND	GND	GND NOT USED (for MU509-65)	GND	GND	NOT USED	GND (for ME909u-521) NOT USED (for ME909u-523)	NOT USED	NOT USED

Pin No.	Interface	Description	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s

NOTE

- N=not supported
- Y=supported
- You need to use a SIM/USIM card in MU509/MU609/ME909u/ME209u-526/ME909s/MU709 and a RUIM card in MC509.
- The electrical features of CMOS 2.6 V interfaces refer to Table 1-4 .
- The electrical features of CMOS 1.8 V interfaces refer to Table 1-5 .
- [1] The firmware does not support these features yet.
- [2] The firmware ME909u-521 supports PCM function and the firmware ME909u-523 does not support PCM function.
- [3] The ME909u-523 module provides two ADC interfaces. ME909u-521 does not support ADC interface at present (the firmware does not support these features yet).
- [4] For ME909s, the power voltage ranges from 3.2 V to 4.2 V.

Table 1-4 Electrical features of CMOS 2.6 V interfaces

Parameter	Description	Minimum Value	Maximum Value	Unit
V_{IH}	High-level input voltage	1.7	2.9	V
V_{IL}	Low-level input voltage	–0.3	0.9	V
V_{OH}	High-level output voltage	2.15	2.6	V
V_{OL}	Low-level output voltage	0	0.45	V

Table 1-5 Electrical features of CMOS 1.8 V interfaces

Parameter	Description	Minimum Value	Maximum Value	Unit
V_{IH}	High-level input voltage	1.17	2.1	V
V_{IL}	Low-level input voltage	–0.3	0.63	V
V_{OH}	High-level output voltage	1.35	1.8	V
V_{OL}	Low-level output voltage	0	0.45	V

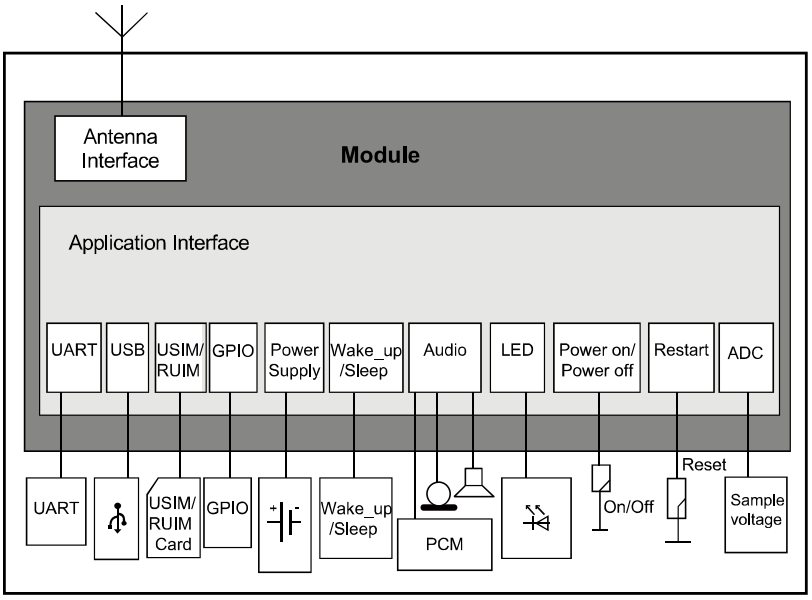
2 LGA Interface Differences

2.1 LGA Interfaces

Huawei 30 mm × 30 mm LGA module provides 145 pads, on which pin 1 to pin 116 are defined as signal pins and pin 121 to pin 145 are defined as heat-dissipation ground pads.

Huawei 30 mm × 30 mm LGA module provides interfaces including power supply, antenna, Universal Serial Bus (USB), Universal Subscriber Identity Module (USIM)/Removable User Identity Module (RUIM), Universal Asynchronous Receiver-Transmitter (UART), audio, Pulse-code Modulation (PCM), Light-emitting Diode (LED), General-purpose I/O (GPIO), WAKEUP_IN, WAKEUP_OUT, SLEEP_STATUS, power on/power off, reset, Joint Test Action Group (JTAG) interfaces, ADC interface and so on.

Figure 2-1 Application block diagram of the 30 mm × 30 mm LGA module



2.2 Control Interface Compatibility Design

2.2.1 Detailed Interface Differences

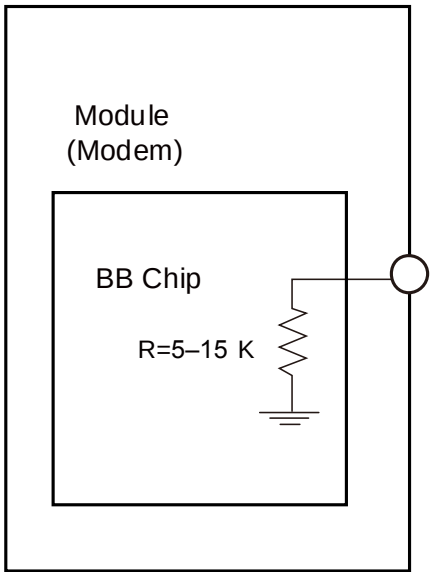
Table 2-1 Differences of the control interfaces

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
11	Control	WAKEUP_IN[1]	CMOS 2.6 V		CMOS 1.8 V				
71		WAKEUP_OUT[2]	CMOS 2.6 V		CMOS 1.8 V				
45		W_DISABLE	GPIO CMOS 2.6 V	CMOS 2.6 V	Reserved				
15		SLEEP_STATUS[3]	Reserved		CMOS 1.8 V				
70		USIM_DET	N	N	N	N	N	Y	Y
81		POWER_ON_OFF	Y	Y	Y	Y	Y	Y	Y
100		RESIN_N	Y	Y	Y	Y	Y	Y	Y

NOTE

- [1]: For ME909s, the pin can be used to wake up the module.
- [2] and [3]: For ME909s, when the module is not in sleep mode, this pin's drive current is 4 mA. **When the module is in sleep mode, this pin's output level is low and drive current smaller than 0.1 mA. The resistance is maintained at 5–15 K, as shown in Figure 2-2 . The output level may be changed if there is a stronger pull-up. It is recommended that customers take Figure 2-4 and Figure 2-5 for reference to design their circuit.**

Figure 2-2 Maintaining the resistance in sleep mode



2.2.2 Control Interface Design Guide

WAKEUP_IN

The host can control LGA module to enter the sleep state through the WAKEUP_IN pin.

When WAKEUP_IN pin is in high level, the module is in the wakeup state.

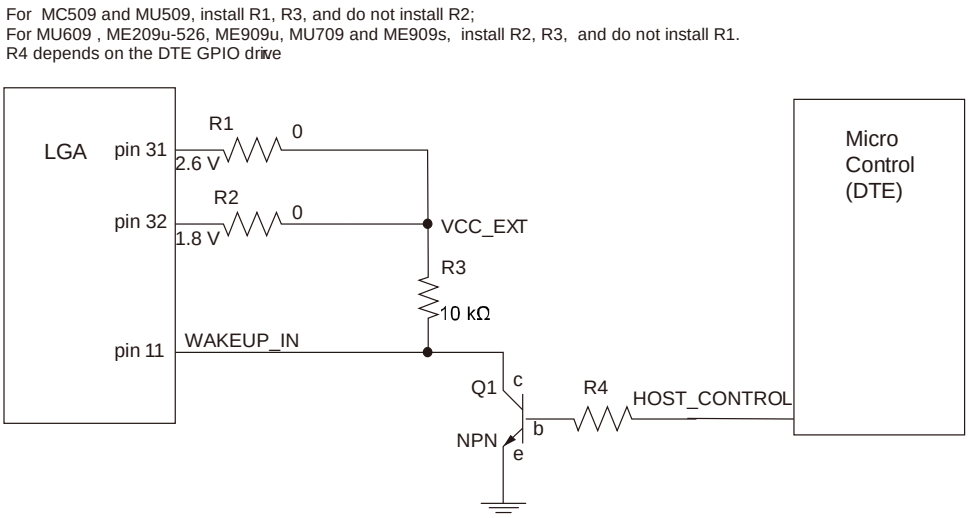
When WAKEUP_IN pin is in low level, MU509/MC509 will be forced into sleep state; MU609/ME209u-526/ME909u/MU709/ME909s will not be forced but be allowed into sleep state instead.

If WAKEUP_IN pin is floated, MU509/MC509 will keep high level internally, while MU609/ME209u-526/ME909u/MU709/ME909s will keep low level internally. For ME209u-526 and ME909u, WAKEUP_IN pin must be connected if you want to normally use the High-Speed UART in future.

Table 2-2 Differences of WAKEUP_IN interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u -526	ME909u	MU709	ME909s
11	Control	WAKEUP_IN	CMOS 2.6 V		CMOS 1.8 V				

Figure 2-3 The recommended connection of WAKEUP_IN pin



NOTE
R4 depends on the actual DTE requirements.

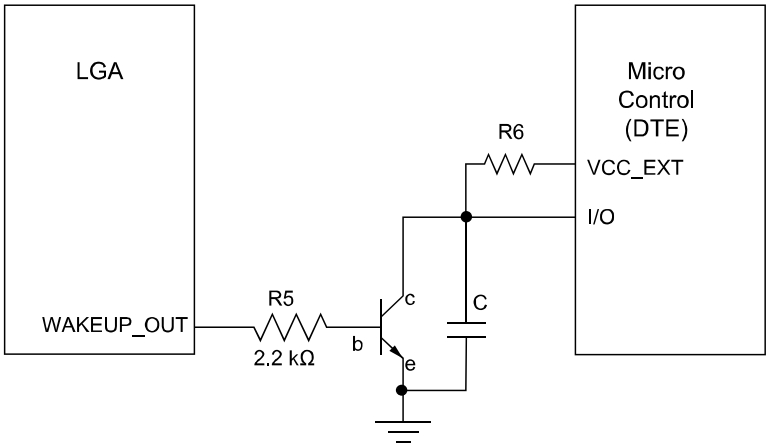
WAKEUP_OUT

The LGA module can wake up the host through the WAKEUP_OUT. To implement compatibility of the signal level, it is recommended that you connect the pin based on the circuit diagram shown in Table 2-3 .

Table 2-3 Differences of WAKEUP_OUT interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
71	Control	WAKEUP_OUT	CMOS 2.6 V		CMOS 1.8 V				

Figure 2-4 The recommended connection of the WAKEUP_OUT pin



NOTE
R6 depends on the actual DTE requirements.

SLEEP_STATUS

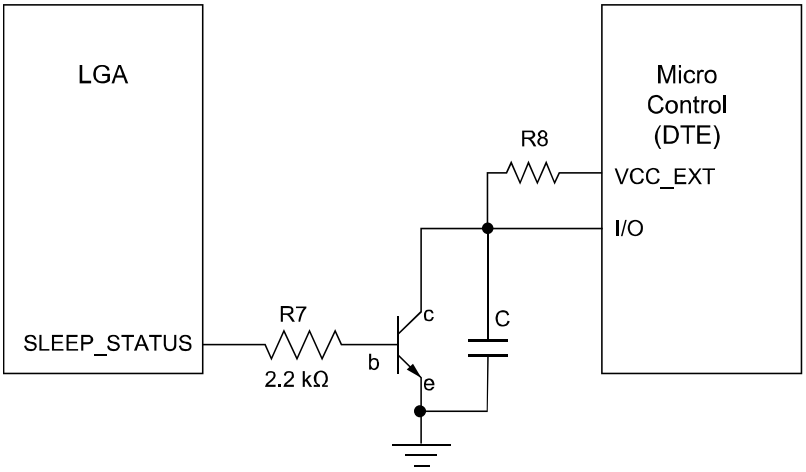
SLEEP_STATUS signal is used to indicate the sleep status of 30 mm × 30 mm LGA module. The external devices can get to know whether the module is in sleep mode by reading SLEEP_STATUS pin.

- When SLEEP_STATUS pin is in high level, 30 mm × 30 mm LGA modules are in wakeup state.
- When SLEEP_STATUS pin is in low level, 30 mm × 30 mm LGA modules are in sleep state.

Table 2-4 Differences of SLEEP_STATUS interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
15	Control	SLEEP_STATUS	Reserved		CMOS 1.8 V				

Figure 2-5 The recommended connection of the SLEEP_STATUS pin



NOTE
R8 depends on the actual DTE requirements.

USIM_DET

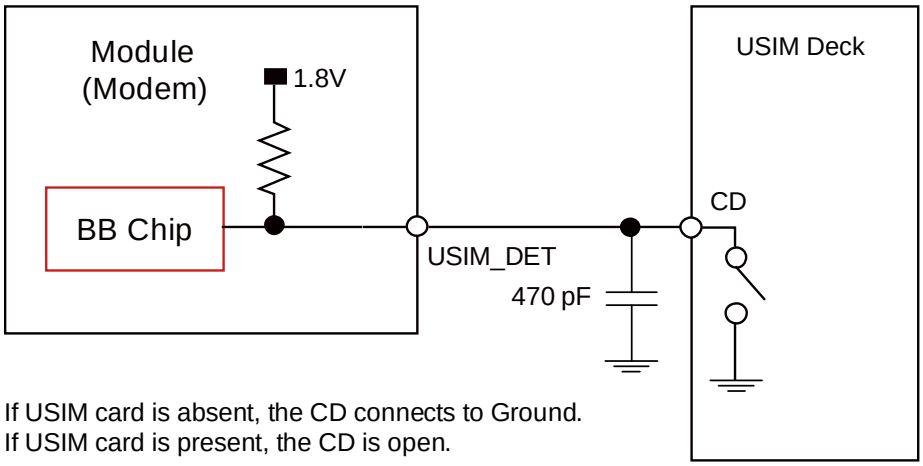
MU709/ME909s support USIM hot swap function.

MU709/ME909s provide an input pin (USIM_DET) to detect whether the USIM card is present or not. This pin is a level trigger pin, and it is internally pulled up. If the module does not support USIM card hot swap, keep USIM_DET floating.

Table 2-5 Function of the USIM_DET pin

No.	USIM_DET	Function
1	High level	USIM card insertion. If the USIM card is present, USIM_DET should be High.
2	Low level	USIM card removal. If the USIM card is absent, USIM_DET should be Low.

Figure 2-6 Connections of the USIM_DET pin



CD is a pin detecting of USIM in the USIM socket, in normal, there will be a detect pin in the USIM socket.

W_DISABLE

Pin 45 works as the W_DISABLE signal by normalization. The MC509 supports this function. MU609, ME209u-526, MU709 and ME909u are now planning this pin for W_DISABLE signal, while this pin is GPIO for MU509.

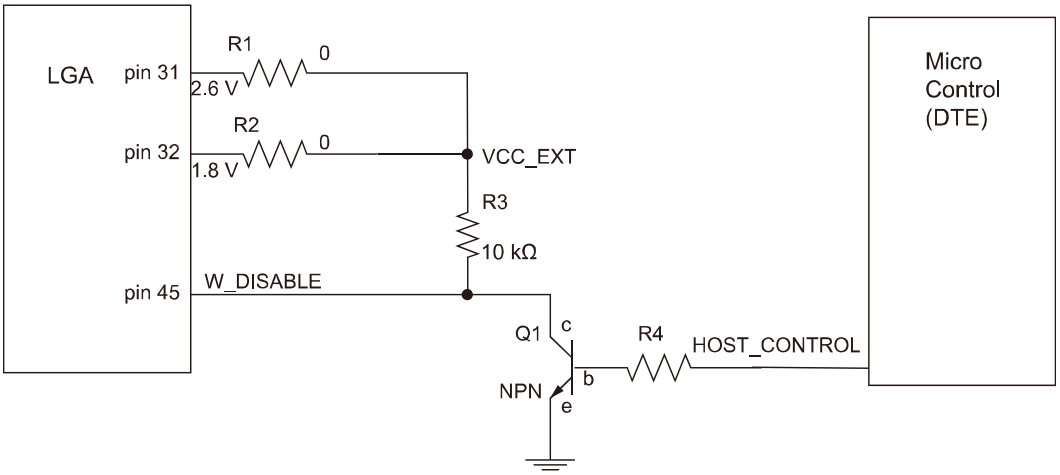
This signal requires an external pull-up resistor, which should be pulled up to VCC_EXT1 (pin 32) or VCC_EXT2 (pin 31). The signal level differs between 30mm × 30mm LGA modules. Therefore, the MC509 uses pin 31 to provide the pull-up power supply and the MU609/ME209u-526/ME909u/MU709/ME909s uses pin 32 to provide the pull-up power supply. The reference circuit diagram is shown in the following figure. A transistor is required to separate this signal from the host control signal.

Table 2-6 Differences of W_DISABLE interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
45	Control	W_DISABLE	GPIO CMOS 2.6 V	CMOS 2.6 V	Reserved				

Figure 2-7 The recommended connection of the W_DISABLE pin

For MC509 and MU509, install R1, R3, and do not install R2;
For MU609, ME209u-526, ME909u, MU709, and ME909s install R2, R3, and do not install R1.
R4 depends on the DTE GPIO driver.



POWER_ON_OFF

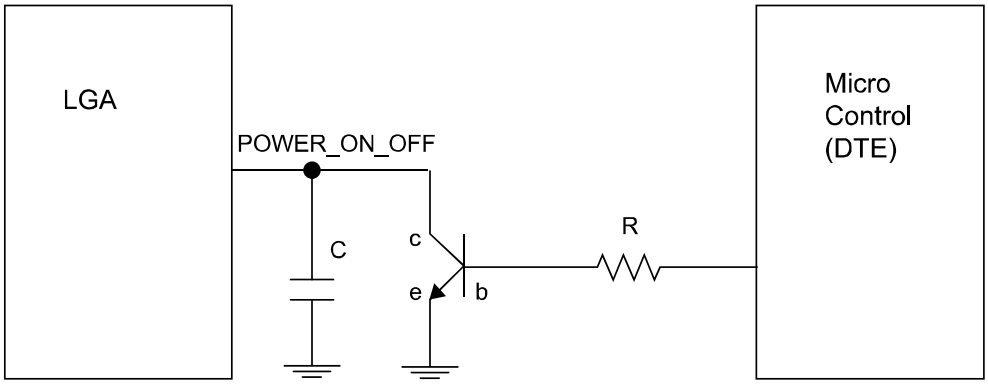
Pin 81 is low active by default and works as the POWER_ON_OFF signal.

- When this pin is pulled down for 0.5s to 1.0s (at least 1.0s for MU709 and ME909s), the module will be powered on.
- When the module works at the normal state, if this pin is pulled down for 3.5s to 4.0s (at least 4.0s for MU709 and ME909s), the module will be powered off.

Table 2-7 Differences of POWER_ON_OFF interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
81	Control	POWER_ON_OFF	Y	Y	Y	Y	Y	Y	Y

Figure 2-8 The recommended connection of the POWER_ON_OFF pin



RESIN_N

Table 2-8 Differences of RESIN_N interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u -526	ME909u	MU709	ME909s
100	Control	RESIN_N	Y	Y	Y	Y	Y	Y	Y

The RESIN_N pin is used to reset the module's system. If the software of module stops responding, you can reset the hardware through the RESIN_N signal as shown in Figure 2-9 . When a low-level pulse is supplied through the RESIN_N pin, the hardware will be reset, and then the software starts powering on the module and reports relevant information according to the actual settings.

Figure 2-9 The recommended connection of the RESIN_N pin

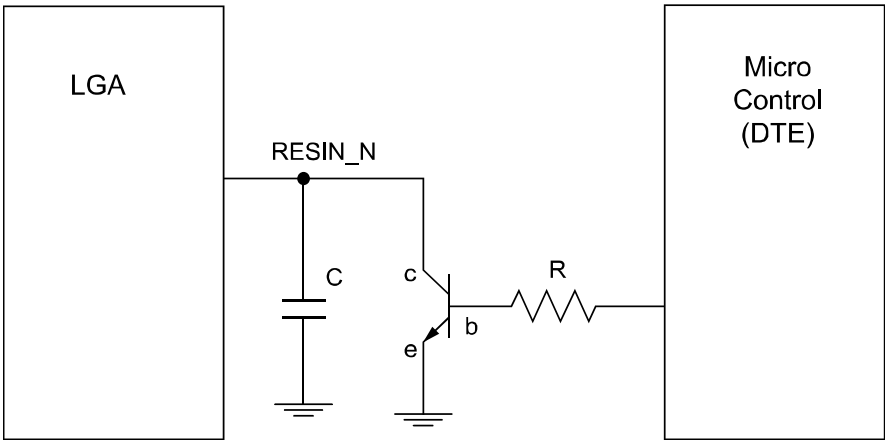
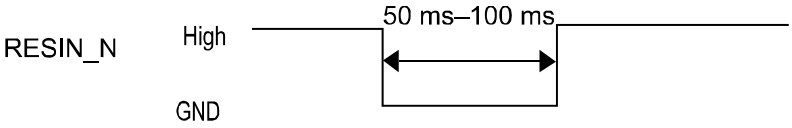


Figure 2-10 Reset pulse timing



NOTE
The RESIN_N pin must not be pulled down for more than 1s.

2.3 Audio Interface Compatibility Design

2.3.1 Detailed Interface Differences

For PCM Audio, MU509, MC509, ME209u-526, ME909u, MU709 and ME909s differ on the level.

For Analog Audio, MU509 and MC509 support Analog Audio, while ME209u-526, ME909u, MU709 and ME909s do not support Analog Audio.

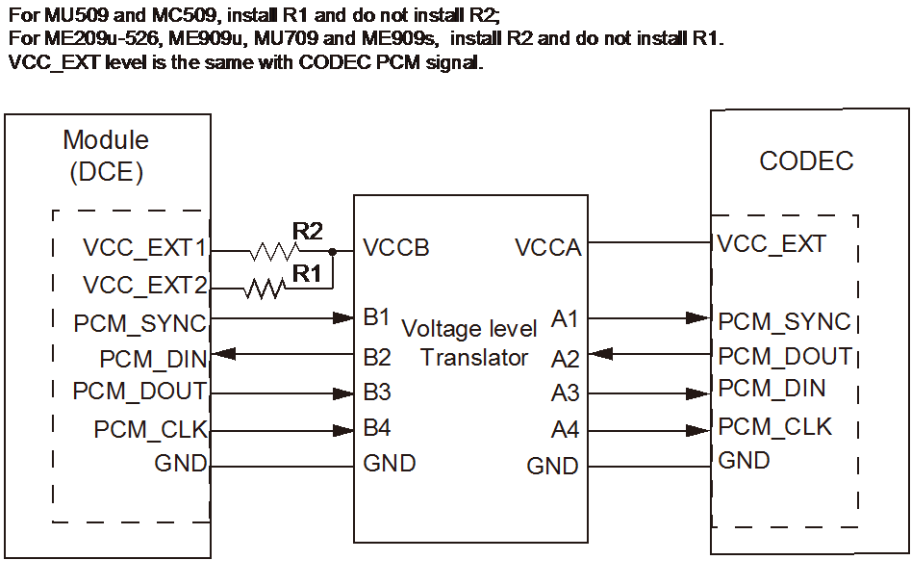
Table 2-9 Differences of the audio interface

Pin No.	Interface	Name	MU509	MC509	MU709	ME209u-526	ME909u	ME909s
5	PCM Audio	PCM_SYNC	CMOS 2.6 V		CMOS 1.8 V	COMS 1.8 V[1]	COMS 1.8 V[1] [2]	CMOS 1.8 V
6		PCM_DIN	CMOS 2.6 V		CMOS 1.8 V			
7		PCM_DOUT	CMOS 2.6 V		CMOS 1.8 V			
8		PCM_CLK	CMOS 2.6 V		CMOS 1.8 V			
38	Analog Audio	MIC2_P	Y	Y	N	N	N	N
39		MIC2_N	Y	Y	N	N	N	N
40		MIC1_P	Y	Y	N	N	N	N
41		MIC1_N	Y	Y	N	N	N	N
96		EAR_OUT_N	Y	Y	N	N	N	N
97		EAR_OUT_P	Y	Y	N	N	N	N
98		SPKR_OUT_P	Y	Y	N	N	N	N
99		SPKR_OUT_N	Y	Y	N	N	N	N

2.3.2 PCM Interface Design Guide

Please note that the different signal level of PCM between MU509/MC509 and ME209u-526/ME909u/MU709/ME909s. The signal of MU509 and MC509 is CMOS 2.6 V and ME209u-526, MU709, ME909u and ME909s are CMOS 1.8 V. Therefore, you must consider compatibility during circuit designing.

Figure 2-11 The recommended connection of the PCM interface in the LGA module



NOTE

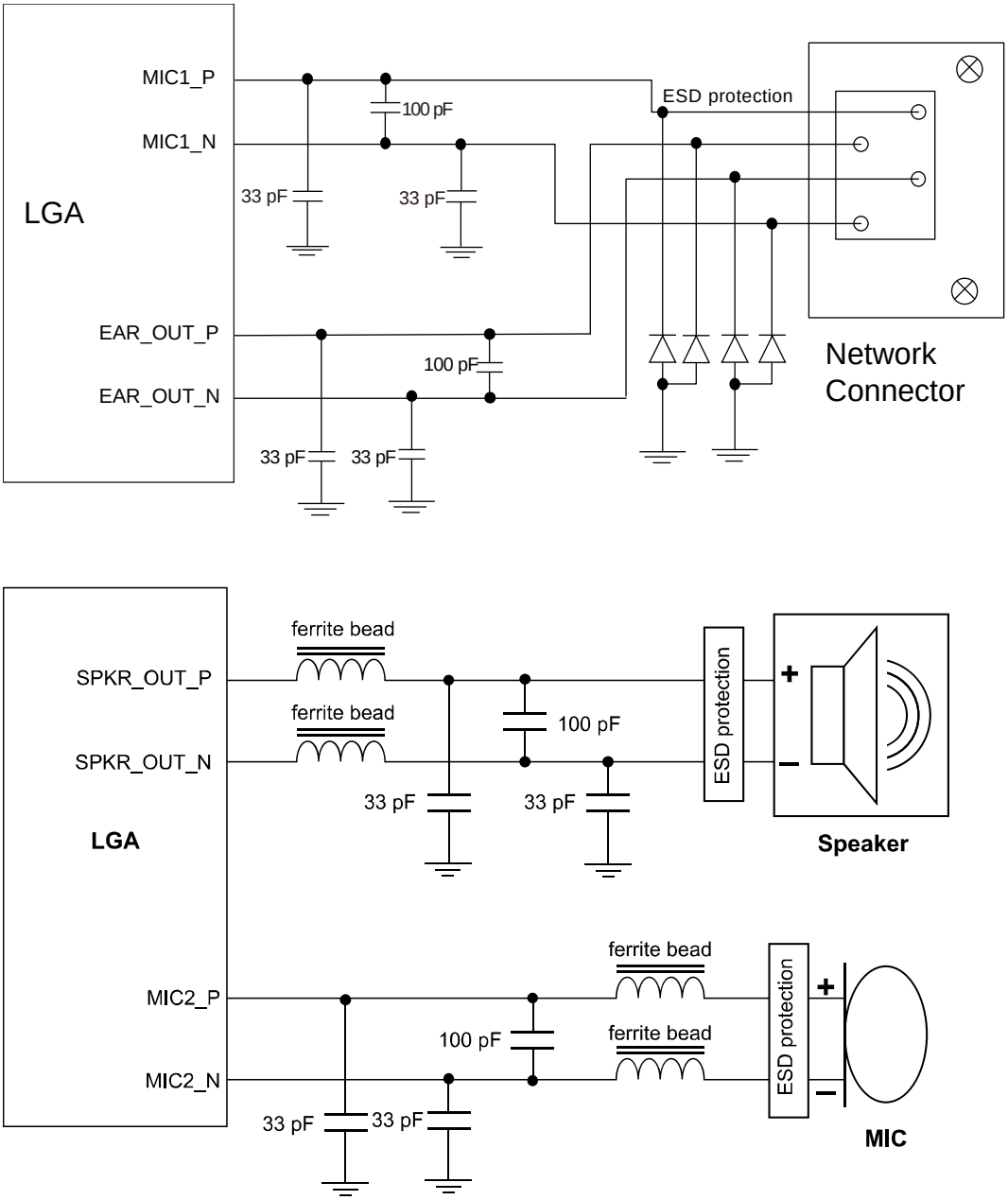
- PCM_SYNC: Output when PCM is in master mode.
- PCM_CLK: Output when PCM is in master mode.
- MU709 and ME909s support both master and slave mode; MC509, MU509 and ME909u-521 only support master mode.
- The firmware of ME909u-523 and ME209u-526 does not support PCM function yet.
- It is recommended that a TVS be used on the related interface, to prevent electrostatic discharge and protect integrated circuit (IC) components.

2.3.3 Analog Interface Design Guide

The ME209u-526, MU709, ME909u and ME909s module do not support the analog audio interface.

MU509 and MC509 module support two channels MIC: one channel EAR and one channel SPEAKER.

Figure 2-12 The circuit diagram of audio interface



2.4 GPIO Interface Compatibility Design

Please note the different signal level of GPIO between MU509/MC509 and MU609/ME209u-526/ME909u/MU709/ME909s. The signal of MU509 and MC509 are CMOS 2.6 V and MU609, MU709, ME209u-526, ME909u and ME909s are CMOS 1.8 V. Therefore, you must consider the compatibility during circuit designing.

Table 2-10 Differences of the GPIO interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
44	GPIO	GPIO	CMOS 2.6 V		N				N
43		GPIO	Reserved	Reserved	Reserved				GPIO
46		GPIO	CMOS 2.6 V		N				GPIO
51		GPIO	CMOS 2.6 V		CMOS 1.8 V				CMOS 1.8 V
55		GPIO	CMOS 2.6 V		CMOS 1.8 V				CMOS 1.8 V
105		GPIO	CMOS 2.6 V		CMOS 1.8 V				CMOS 1.8 V
109		GPIO	CMOS 2.6 V		CMOS 1.8 V				CMOS 1.8 V
113		GPIO	CMOS 2.6 V		CMOS 1.8 V				CMOS 1.8 V

NOTE

- For ME909s, when the GPIO interface is used for input, the module will not respond in sleep mode (it will resume response after being waken up from sleep mode by the WAKEUP_IN pin) and the module is configured to pull-down inside. In sleep mode, the pull-down resistance is 5–15 K. For the peripheral circuits, see Figure 2-13 .
- For ME909s, when the GPIO interface is used for output and the module is not in sleep mode, the drive current is 4 mA. When the module is in sleep mode, the drive current is smaller than 0.1 mA. The resistance is maintained at 5–15 K, as shown in Figure 2-14 . The output level may be changed if there is a stronger pull-up or pull-down. For the peripheral circuits, see Figure 2-15 .

Figure 2-13 Reference peripheral circuits when the GPIO interface is used for input

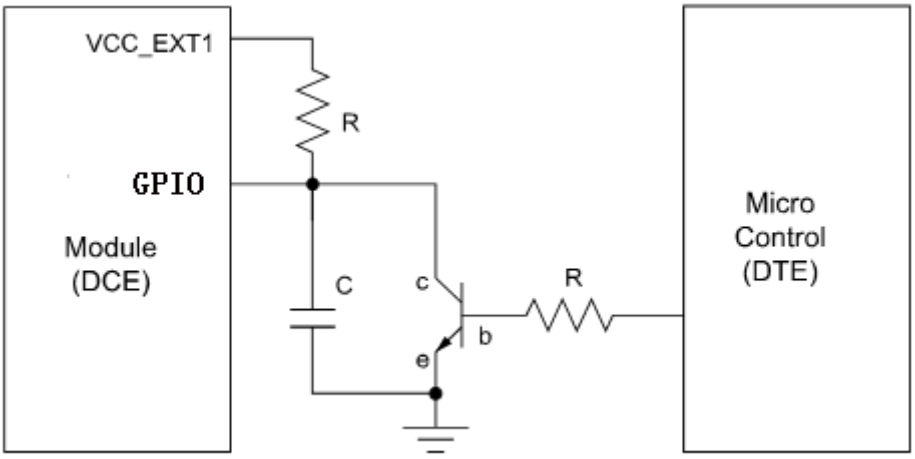


Figure 2-14 Maintaining the resistance in sleep mode

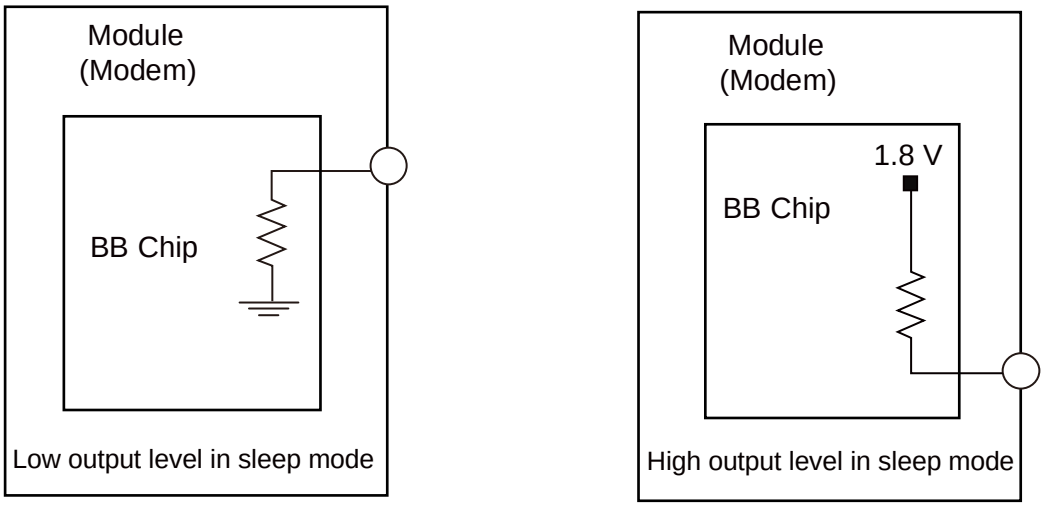


Figure 2-15 Reference peripheral circuits when the GPIO interface is used for output

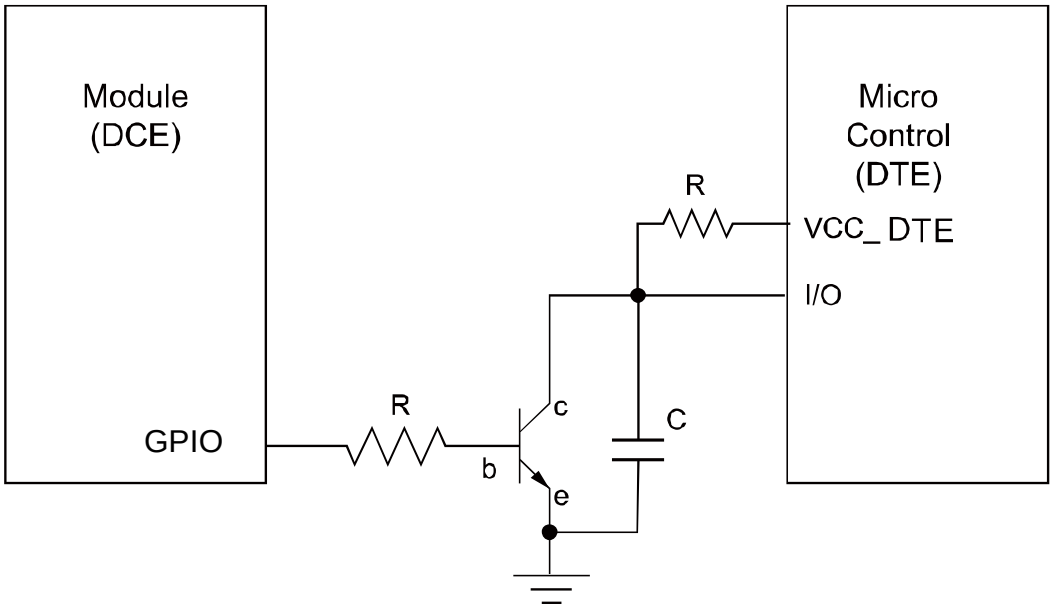
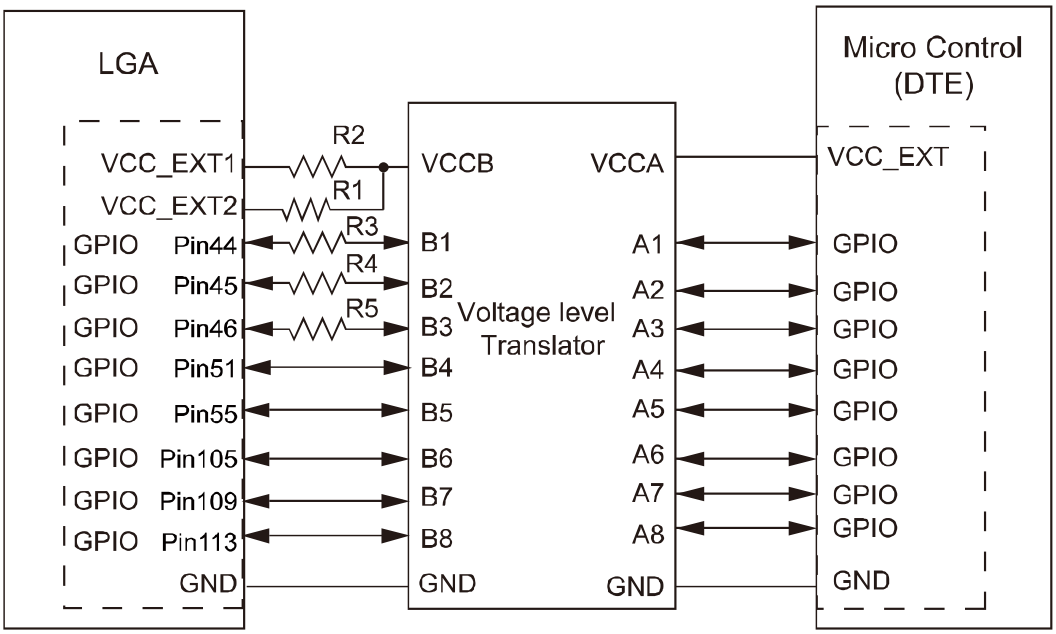


Figure 2-16 The recommended connection of the GPIO pin

For MU509, install R1,R3,R4,R5 and do not install R2;
For MC509, please install R1,R3,R5, and donot install R2 and R4, design pin 45 referring to the design of W_DISABLE;
For MU609, ME209u-526, ME909u ,ME909s and MU709, install R2 and do not install R1,R3,R4,R5.
VCC_EXT level is the same with DTE GPIO signal.
if MU509 does not need 8 GPIOs, please design pin 45 referring to the design of W_DISABLE in order to be compatible with MC509, MU609, ME209u-526,ME909s, MU709 and ME909u.



NOTE
The pin 45 of the MU609, ME209u-526, MU709 and ME909u are planning for W_DISABLE.

2.5 Antenna Interface Compatibility Design

2.5.1 Detailed Interface Differences

Please note that the difference of antenna among 30 mm × 30 mm LGA modules. MU509 only supports MAIN_ANT. MC509, MU609 and ME909u support MAIN_ANT, AUX_ANT (Diversity) and GPS_ANT. ME209u-526, MU709 and ME909s support MAIN_ANT and AUX_ANT (Diversity).

Table 2-11 Differences of the antenna interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
107	Antenna	MAIN_ANT	Y	Y	Y	Y	Y	Y	Y
111		GPS_ANT	N	Y	Y	N	Y	N	N
115		AUX_ANT	N	Y	Y	Y	Y	Y	Y

2.5.2 Antenna Interface Design Guide

To implement compatibility among the Huawei 30 mm × 30 mm LGA modules, pay attention to antenna interfaces pin 107 (MAIN_ANT), pin 111 (GPS_ANT), and pin 115 (AUX_ANT).

Pay attention to the interface differences among the MU509 and other 30 mm × 30 mm LGA modules.

Table 2-12 Differences of the antenna interface in pad size and function

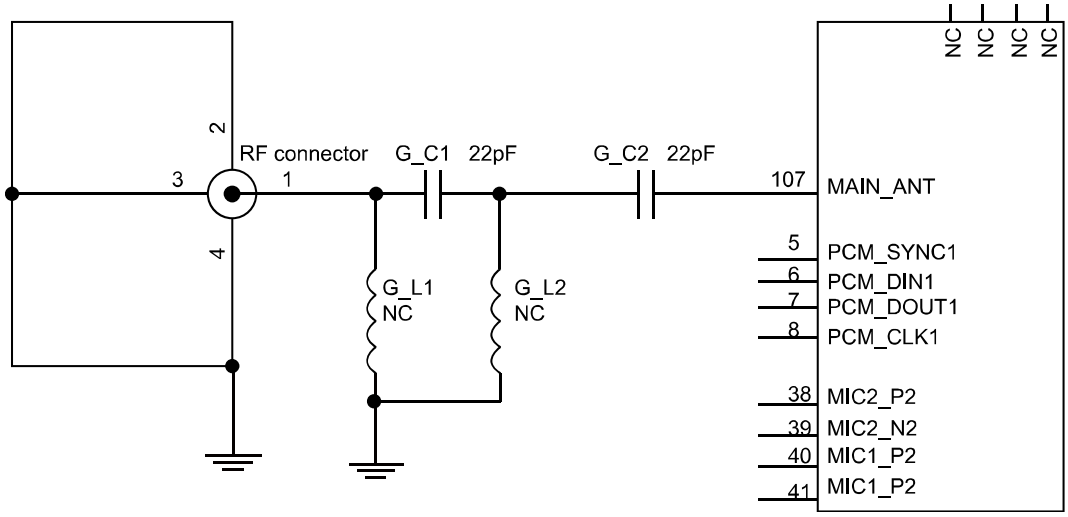
<table>
<tr><th>Pin No.</th><th>Interface</th><th>Name</th><th>MU509</th><th>MC509</th><th>MU609</th><th>ME909u</th><th>ME209u-526</th><th>MU709</th><th>ME909s</th></tr>
<tr><td rowspan="2">107, 111 and 115</td><td rowspan="2">Antenna interface</td><td>ANT pad size</td><td colspan="2">1.5 mm × 1.0 mm</td><td colspan="5">1.02 mm × 0.82 mm</td></tr>
<tr><td>ANT function</td><td>Main (pin 107)</td><td colspan="3">Main (pin 107),
AUX (pin 115),
GPS (pin 111)</td><td colspan="2">Main (pin 107),
AUX (pin 115)</td><td>Main (pin 107),
AUX (pin 115)</td></tr>
</table>

RF Signal Trace in the Main Board Design of Customers

It is recommended that you design antenna interfaces as follows:

- The antenna signal trace must be as short as possible, and controlled with 50 Ω impedance.
- The antenna interfaces pin 107, pin 111, and pin 115 should be also controlled with 50 Ω impedance.
- A π matching network must be reserved for radio frequency (RF) trace between output pins of MAIN_ANT, AUX_ANT, and GPS_ANT and antenna interfaces. There is an example of the matching network for MAIN_ANT as shown in Figure 2-17 .The components of G_C1, G_L1, and G_L2 compose a π matching network. The G_C2 is for DC blocking and matching design. The matching network for AUX_ANT and GPS_ANT are the same as the MAIN_ANT.

Figure 2-17 The matching network for MAIN_ANT



CAUTION

To implement 50 Ω impedance, the designer should adjust the components G_C1, G_L1, G_L2 and G_C2 shown in the preceding figure as required.

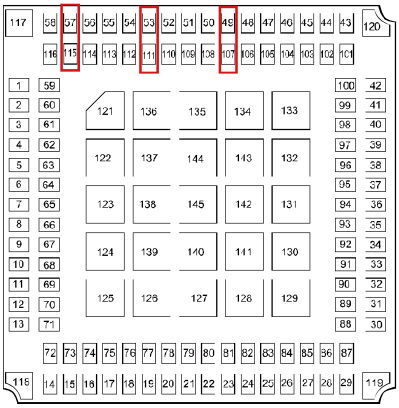
RF Interface Design for Modules

The recommended RF Pad design is shown as follows for different modules selection.

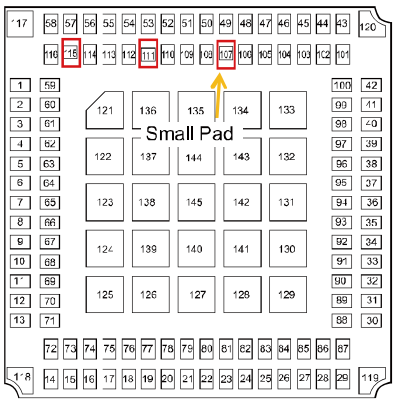
Please note that the Pad and RF trace design changes in the main board.

Figure 2-18 RF Pad design for different modules selection (Top view of LGA)

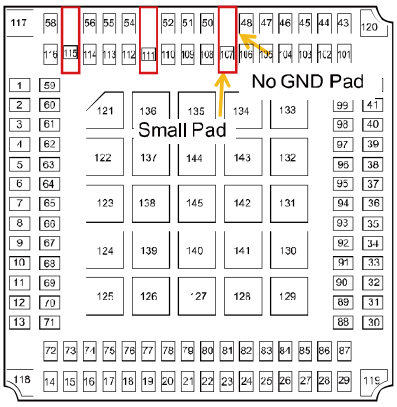
MU509-b/MU509-c/MU509-g /MC509



MU609/ME909u-521

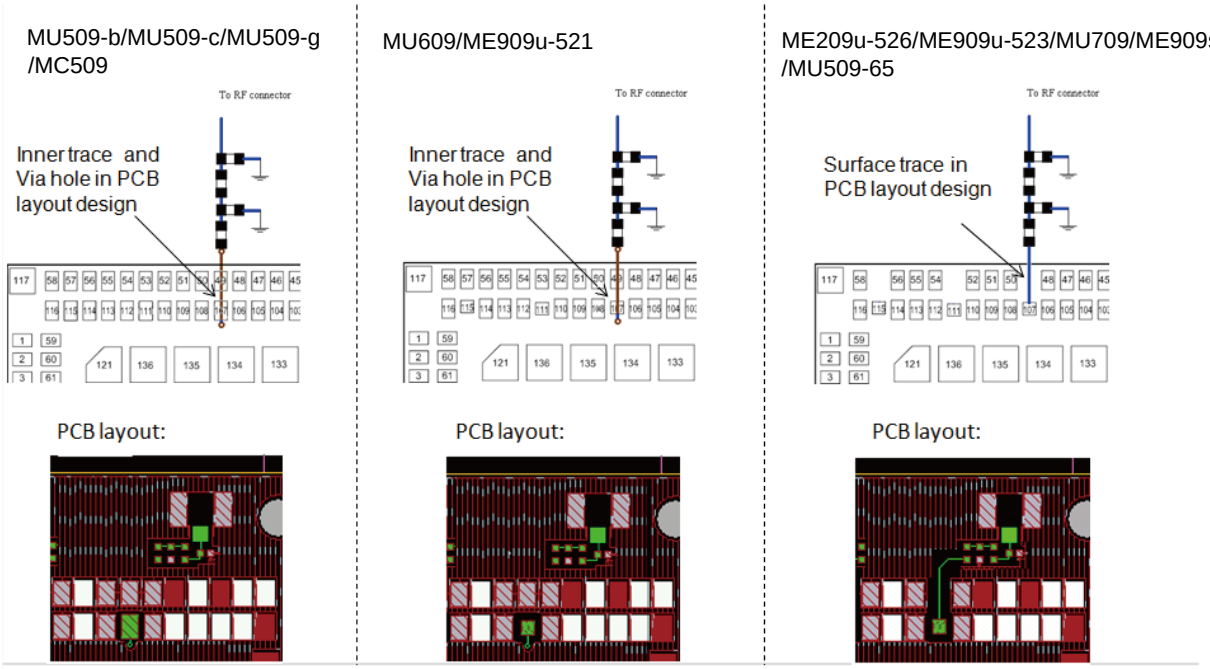


ME209u-526/ME909u-523/MU709 /ME909s/MU509-65



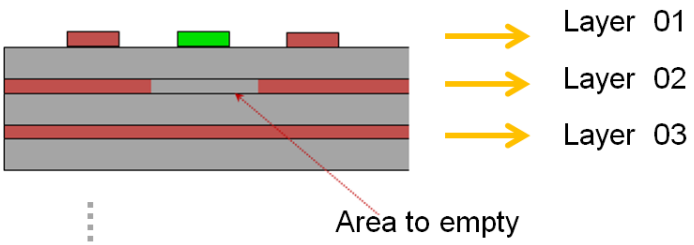
RF Trace Design

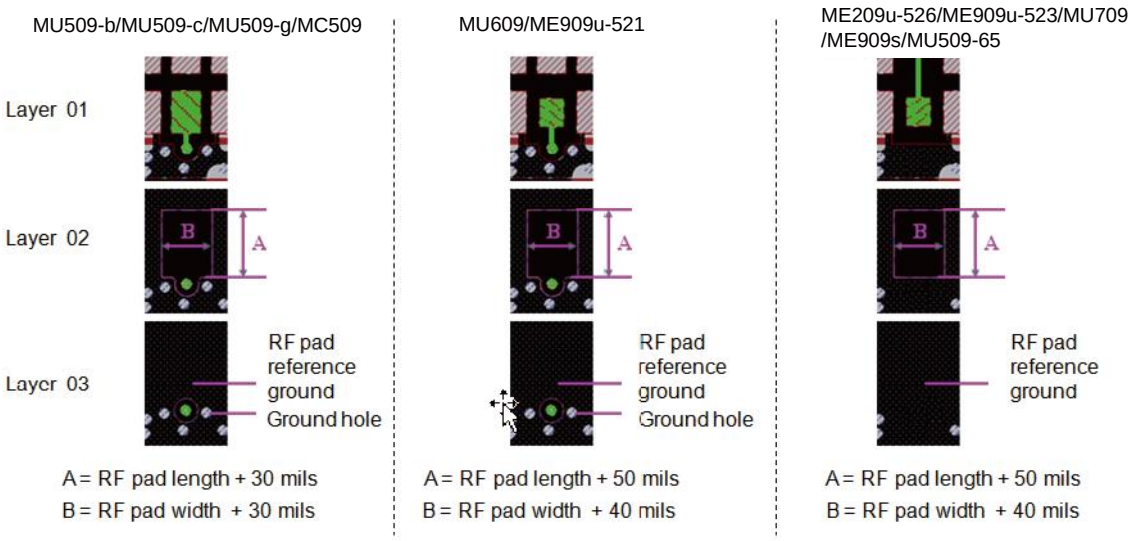
Take pin 107 for example (Top view of LGA and the main board):



RF Pad Design

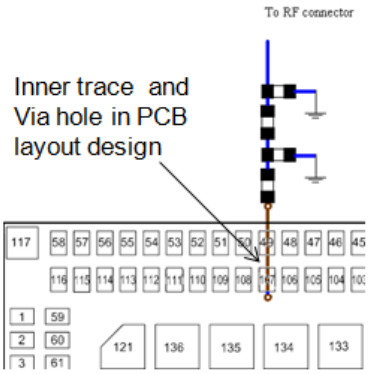
Take pin 107 for example:



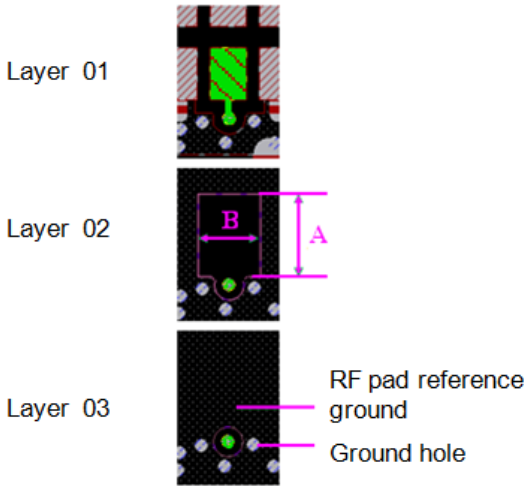


RF Interface for Module Migration Design

- MU509/MC509, MU609/ME909u-521, and ME209u-526/ME909u-523/MU709/ME909s/MU509-65 modules need to be compatible. We recommend that the RF interface design follow the design of MU509/MC509.



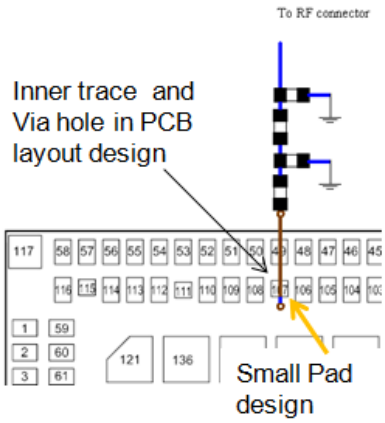
Top view of LGA and main board



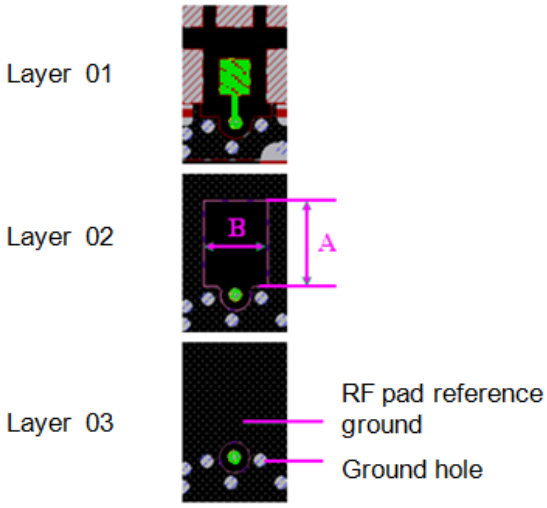
A = RF pad length + 30 mils

B = RF pad width + 30 mils

- MU609/ME909u-521 and ME209u-526/ME909u-523/MU709/ME909s/MU509-65 modules need to be compatible. We recommend the RF interface design follow the design of MU609/ME909u-521.



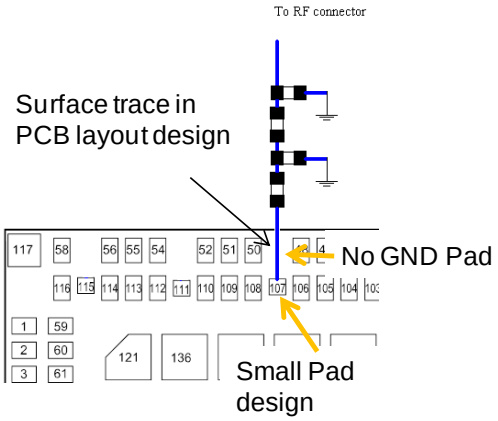
Top view of LGA and main board



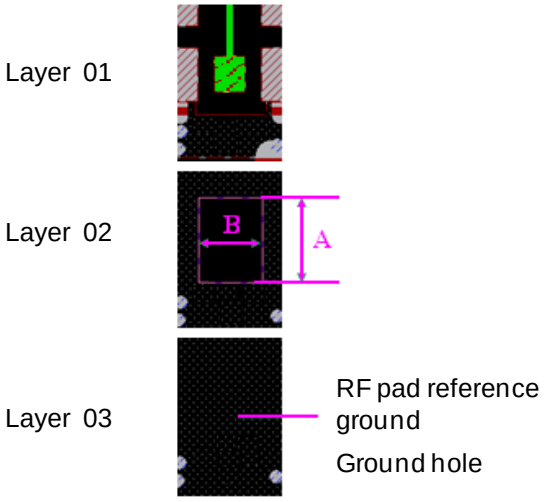
A = RF pad length + 50 mils

B = RF pad width + 40 mils

- ME209u-526/ME909u-523/MU709/ME909s/MU509-65 module need to be compatible. We recommend the RF interface design follow the design of ME209u-526/ME909u-523/MU709/ME909s/MU509-65.



Top view of LGA and main board



A = RF pad length + 50 mils

B = RF pad width + 40 mils

NOTE

- We recommend the RF interface design for different modules can accord to their own reference design.
- We recommend digging the adjacent layer below the RF pad for better RF trace impedance control.
- The pin 111 and pin 115 signal trace layout can be the same as pin 107 (MAIN_ANT).

2.6 VCC_EXT Interface Compatibility Design

Because the signal level of MC509 and MU509 is different from MU609, MU709, ME209u-526, ME909u and ME909s, there are two output supplies as for reference level. One is VCC_EXT2 (2.6 V), the other is VCC_EXT1 (1.8 V).

Table 2-13 Differences of the VCC_EXT interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
31	VCC_EXT	VCC_EXT2	2.6 V	2.6 V	N	N	N	N	N
32		VCC_EXT1	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V

2.7 VBAT Interface Compatibility Design

2.7.1 Detailed Interface Differences

The VBAT voltage ranges from 3.3 V to 4.2 V, and it ranges from 3.2 V to 4.2 V for ME909s, with a typical value being 3.8 V. The 30 mm × 30 mm LGA module provides two VBAT pads.

When the 30 mm × 30 mm LGA module works in the GSM mode, the peak current can reach 2.75 A. To ensure that the module works normally, place a large-capacity capacitor (1.1 mF is the best) near VBAT pads. This ensures that the VBAT voltage is not lower than 3.3 V, and for ME909s, it is not lower than 3.2 V.

All the 30 mm × 30 mm LGA modules must be installed with a large-capacity capacitor on the VBAT. Furthermore, five 220 µF or above energy storage capacitors are connected in parallel at the power interface of the LGA module (VBAT Pin). But for MC509, a 220 µF or above energy storage capacitors in parallel are enough.

Table 2-14 Differences of capacitors in parallel at the VBAT Pin

Pin No.	Interface	Name	MC509	MU509	MU609	ME209u-526	ME909u	MU709	ME909s
12 and 13	Power interface	VBAT (3.3 V–4.2 V) VBAT (3.2 V–4.2 V) is only for ME909s	A 220 µF capacitor needed	Five 220 µF capacitors needed					

2.7.2 VBAT Interface Design Guide

It is recommended that you add ferrite beads and five 220 µF capacitors (a 220 µF capacitor for MC509) are connected in parallel at VBAT pin to the power circuit. The diagram of recommended circuit is shown in the following figures.

Figure 2-19 Recommended power circuit of MU509/MU609/ME209u-526/ME909u/MU709/ME909s module

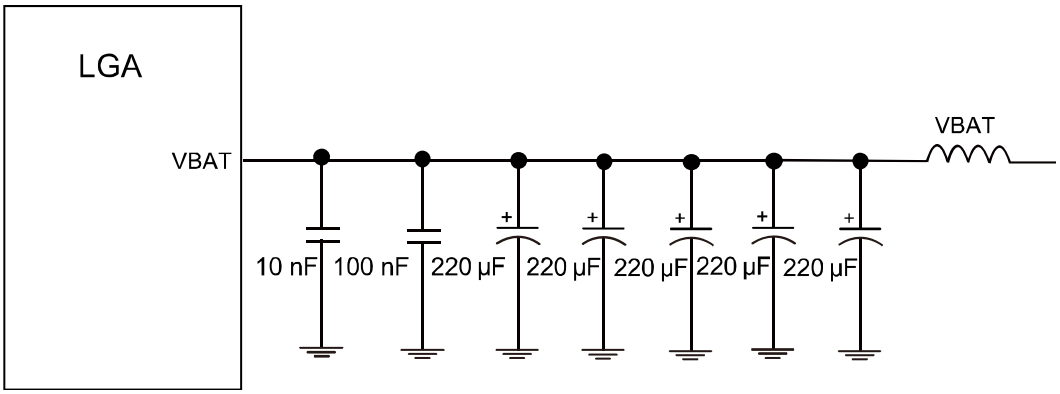
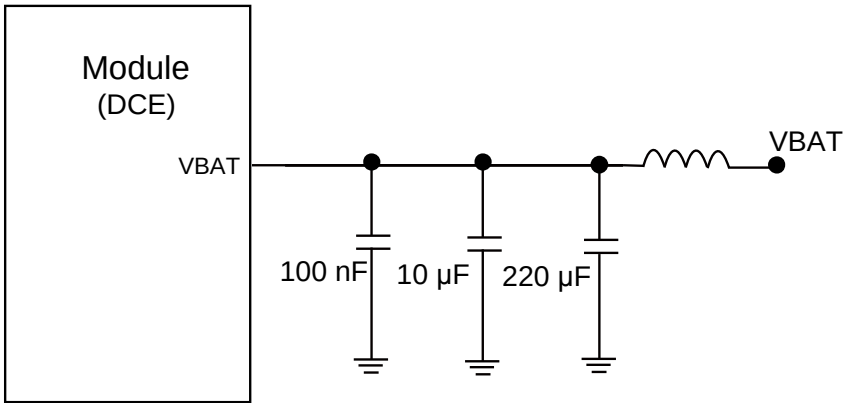


Figure 2-20 Recommended power circuit of MC509 module



2.8 JTAG Interface Compatibility Design

2.8.1 Detailed Interface Differences

Please note that JTAG level (CMOS 2.6 V) of MC509 is different from JTAG level (CMOS 1.8 V) of MU509/MU609/ME209u-526/ME909u/MU709/ME909s.

Table 2-15 Differences of the JTAG signal

Pin No.	Interface	Name	MC509	MU509	MU609	ME209u-526	ME909u	MU709	ME909s
30	JTAG	JTAG_TMS	CMOS 2.6 V	CMOS 1.8 V					
36		JTAG_TRST_N							
42		JTAG_TCK							

Pin No.	Interface	Name	MC509	MU509	MU609	ME209u-526	ME909u	MU709	ME909s
72		JTAG_TDO							
87		JTAG_TDI							
93		JTAG_RTCK		CMOS 1.8 V				Reserved	CMOS 1.8 V
14		PS_HOLD	CMOS 1.8 V	CMOS 1.8 V					N
100/47		RESIN_N/JTAG_SRST_N	CMOS 1.8 V (pin 100)			**JTAG_SRST_N (pin 47) reset for JTAG debugging**		CMOS 1.8 V (pin 100)	RESIN_N (pin 100)

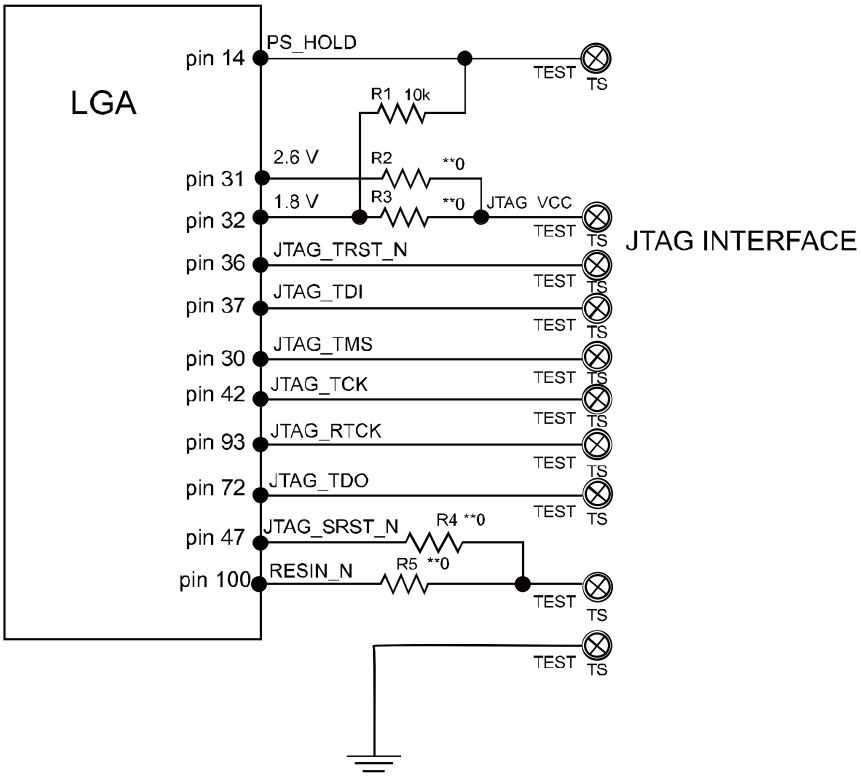
2.8.2 JTAG Interface Design Guide

To facilitate fault location, it is recommended that you lead out JTAG signals from test points. The LGA module must be reserved with JTAG test point interfaces for fault analysis and location. The JTAG interface signals include the following signals. Arrange test points according to the following relationship.

The following figure shows the connections of JTAG signal pins.

Figure 2-21 Circuit of the JTAG interface

When you want 30 mm×30 mm LGA module in JTAG mode, please Install R1;
When you want 30 mm×30 mm LGA module in normal mode, please do not install R1;
For MC509, install R2 and do not install R3;
For MU509/MU609/ME209u-526/ME909u/MU709/ME909s, install R3 and do not install R2



For ME209u-526/ME909u, install R4 and do not install R5;
For MC509/MU509/MU609/MU709/ME909s, install R5 and do not install R4

2.9 UART Interface Compatibility Design

2.9.1 Detailed Interface Differences

Please note that the different signal level of UART between MU509/MC509 and MU609/ME209u-526/ME909u/MU709/ME909s. The signal level of MU509/MC509 is CMOS 2.6 V and MU609/MU709/ME209u-526/ME909u/ME909s is CMOS 1.8 V. Therefore, you must consider compatibility during circuit designing.

ME209u-526 and ME909u only support two 4-wire line UARTs and one 2-wire UART (only for debugging), and do not support 8-wire line UART.

For ME909s, the UART cannot wake up the module from the sleep status, and you can pull up the WAKEUP_IN signal for 1s instead.

Table 2-16 Differences of the UART interface

Pin No.	Interface	Name	MU509	MC509	MU609	MU709	ME209u-526	ME909u	ME909s
73	UART	UART0_DSR	CMOS 2.6 V		CMOS 1.8 V		N		CMOS 1.8 V
74		UART0_RTS	CMOS 2.6 V		CMOS 1.8 V				
75		UART0_DCD	CMOS 2.6 V		CMOS 1.8 V		N		CMOS 1.8 V
76		UART0_TX	CMOS 2.6 V		CMOS 1.8 V				
77		UART0_RING	CMOS 2.6 V		CMOS 1.8 V		N		CMOS 1.8 V
78		UART0_RX	CMOS 2.6 V		CMOS 1.8 V				CMOS 1.8 V
79		UART0_DTR	CMOS 2.6 V		CMOS 1.8 V		N		CMOS 1.8 V
80		UART0_CTS	CMOS 2.6 V		CMOS 1.8 V				CMOS 1.8 V
1		UART1_TX	N	N	CMOS 1.8 V for debugging		CMOS 1.8 V		N
2		UART1_RTS	N	N	N	N	CMOS 1.8 V		N
3		UART1_CTS	N	N	N	N	CMOS 1.8 V		N
4		UART1_RX	N	N	CMOS 1.8 V for debugging		CMOS 1.8 V		N
28		UART2_TX	Reserved				CMOS 1.8 V for debugging		
29		UART2_RX	Reserved				CMOS 1.8 V for debugging		

2.9.2 UART Interface Design Guide

CAUTION

Besides compatibility of the UART, designers must consider the time sequence of signals. The UART signals externally connected with the LGA module must be transmitted at least 3s after the LGA module is powered on. Otherwise, a sink current occurs and the LGA module may be improperly powered on.

Figure 2-22 The recommended connection of the UART0 interface in the module (DCE) with the host (DTE)

For MU509 and MC509, install R1,R3,R4,R5,R6, and do not install R2;
For MU609, MU709 and ME909s, install R2,R3,R4,R5,R6, and do not install R1.
For ME209u-526 and ME909u, install R2, and do not install R1,R3,R4,R5,R6.
VCC_EXT level is the same with DTE UART signal.

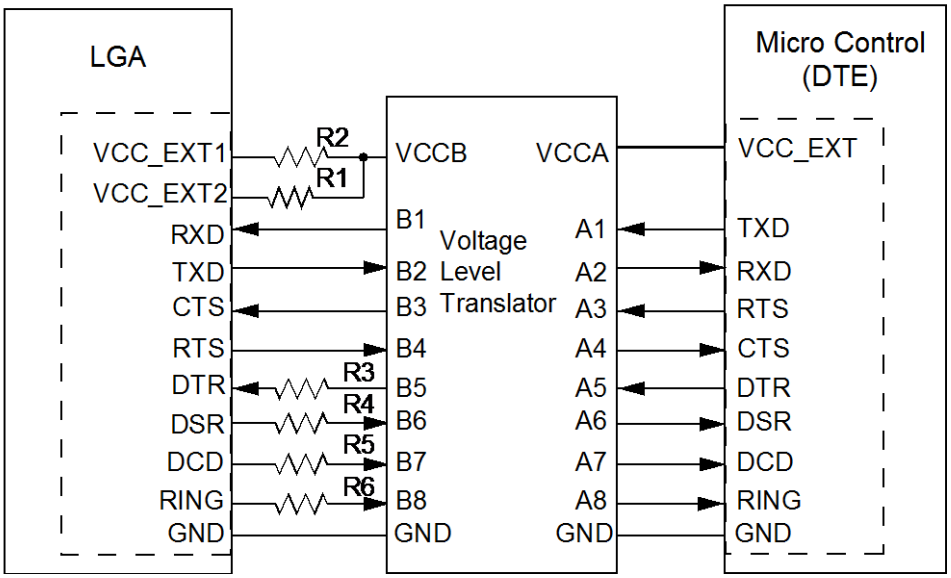


Figure 2-23 The recommended connection of the UART1 interface in the module (DCE) with the host (DTE)

For MU509, MC509 and ME909s, do not install R1,R2,R3,R4,R5,R6;
For MU609 and MU709 for debugging, install R2,R3,R4, and do not install R1,R5,R6.
For ME209u-526 and ME909u, install R2, R3,R4,R5,R6, and do not install R1.
VCC_EXT level is the same with DTE UART signal.

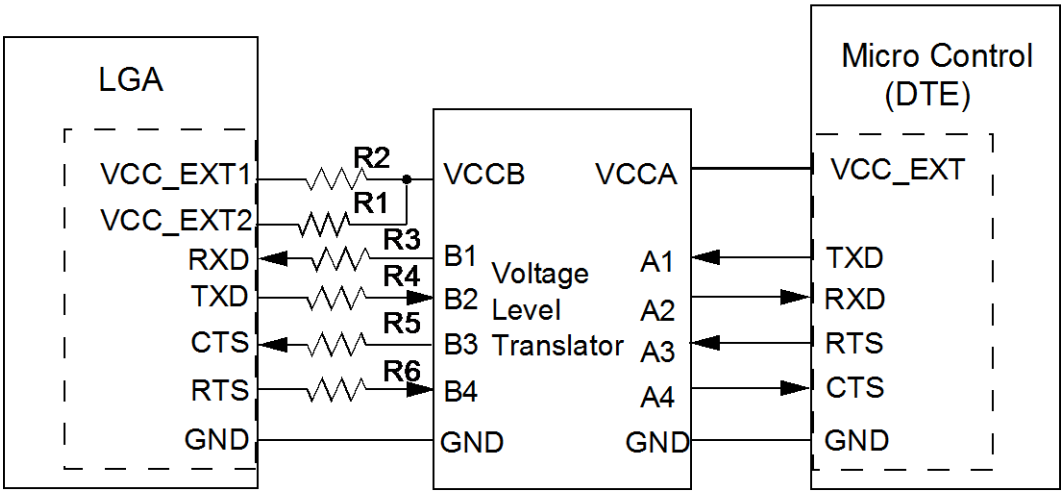
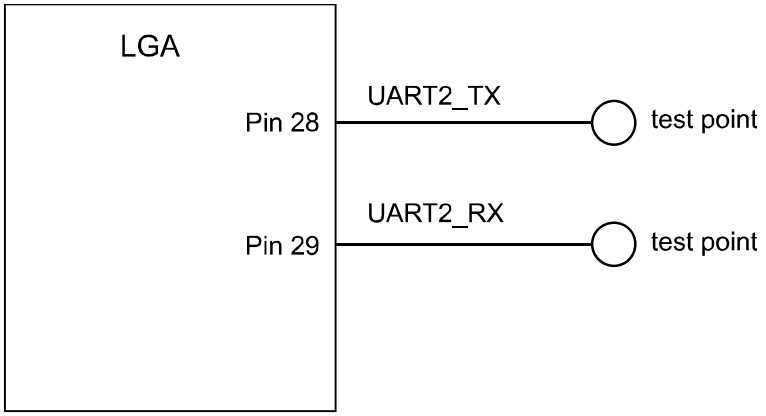


Figure 2-24 Circuit diagram of the UART2 interface (only for debugging)



2.10 USB Interface Compatibility Design

2.10.1 Detailed Interface Differences

Please note that only MU609, MU709, ME209u-526, ME909u and ME909s support USB 2.0 High Speed. MC509 and MU509 do not support USB 2.0 High Speed.

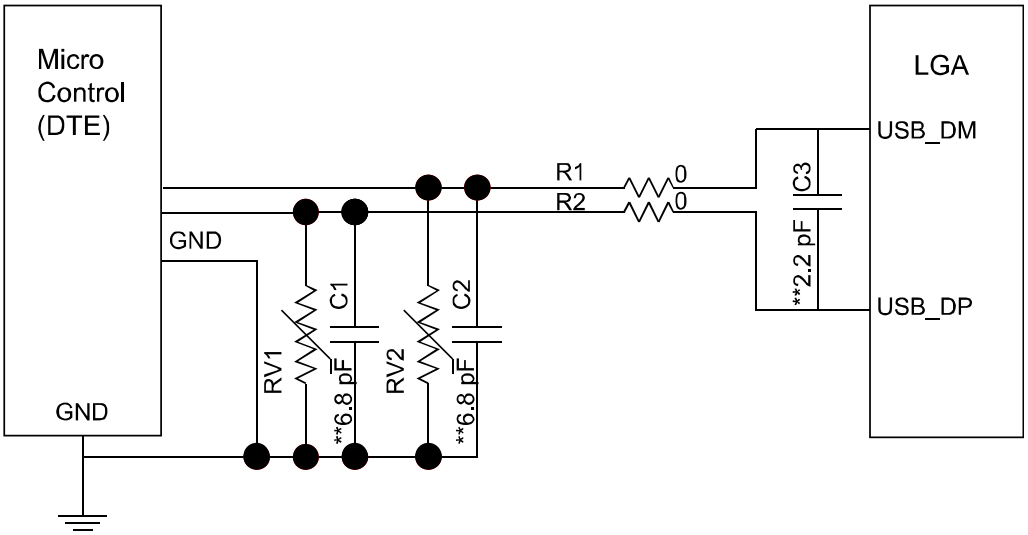
Table 2-17 Differences of the USB interface

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
85	USB	USB_DM	USB 2.0 Full Speed		USB 2.0 High Speed				
86		USB_DP	USB 2.0 Full Speed		USB 2.0 High Speed				

2.10.2 USB Interface Design Guide

The following figure shows recommended circuit of USB interface.

Figure 2-25 Recommended circuit of USB interface



Requirements for USB signal layout and traces:

1. USB_DM and USB_DP are required to control the differential impedance 90 Ω.
2. R1 and R2 are ready for dealing with impedance matching. You can adjust the value of R1 or R2 in order that the differential impedance of the USB signal should be 90 Ω.
3. The length of the gap between USB_DM and USB_DP should not exceed 5mil.
4. The USB differential signal trace must be as short as possible, and laid out away from high-speed clock signals and other periodic signals as far as possible.
5. Minimize through-holes and turning angles on the USB signal trace to reduce signal reflection and impedance change.
6. Do not route the USB signal trace under the following components: crystal, oscillator, clock circuit, electromagnetic component, and IC that uses or generates clocks.
7. Avoid stubs on the USB signal trace because stubs generate reflection and affect the signal quality.
8. Route the USB signal trace on a complete reference plane (GND) and avoid crossing inter-board gaps because inter-board gaps cause a large reflow channel area and increase inductance and radiation. In addition, avoid signal traces on different layers.
9. The USB signal trace must be far away from core logical components because the high current pulse is generated during the state transitions process of core components may impose interference on signals.
10. The USB signal trace must be far away from board edges with a minimum distance of 20 × h (h indicates the vertical distance between the trace and the reference layer) to avoid signal radiation.
11. C1 and C2 are ready for dealing with filter differential mode interference and C3 is ready for dealing with filter common mode interference. You can choose the value of the C1, C2 and C3 according to the actual PCB which is integrated 30 mm×30 mm LGA Module.

NOTE
"**" means do not install at first, but C1, C2 and C3 need to reserve the capacitor pads in order to deal with filter common and differential mode interference.

2.11 LED Interface Compatibility Design

2.11.1 Detailed Interface Differences

Table 2-18 Differences of LED control signal

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
91	LED	LED_STATUS	Y	Y	Reserved				
101		LED_MODE	Y	Y	Y	Y	Y	Y	Y

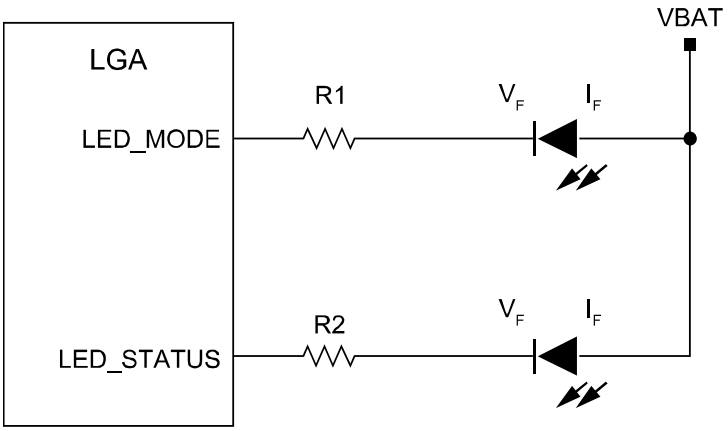
2.11.2 LED Interface Design Guide

Pin 91 and pin 101 are worked as LED control signals, which are the current sink type; and the drive strength is 10 mA.

For the pins of current sink type, it is recommended that you connect the pins based on the circuit diagram shown in the following figure. R1 and R2 can be adjusted according to the actual LED brightness. The VCC voltage must not exceed VBAT +0.5 V; otherwise, the internal chip of a module may be damaged. It is recommended that you use the VBAT as the VCC.

For the details about the LED working status, you can refer the product's hardware guide.

Figure 2-26 Circuit of the LED interface



2.12 ADC Interface Compatibility Design

Table 2-19 Differences of ADC signal

Pin No.	Interface	Name	MU509	MC509	MU609	ME209u-526	ME909u	MU709	ME909s
102	ADC	ADC_1	N	N	N	Y	Y[1]	N	Y
104		ADC_2	N	N	N	Y	Y[1]	N	Y

NOTE
[1]: The ME909u-523 module provides two ADC interfaces. ME909u-521 does not support ADC interface at present (the firmware does not support these features yet).

3 Mechanical Specifications Compatibility Design Guide

3.1 Dimension Differences

Table 3-1 shows the dimension differences of Huawei 30 mm × 30 mm LGA modules.

It is recommended that the reserved height is 2.65 mm ± 0.20 mm (height of MC509, which is the highest of Huawei 30 mm × 30 mm LGA modules) for compatibility design.

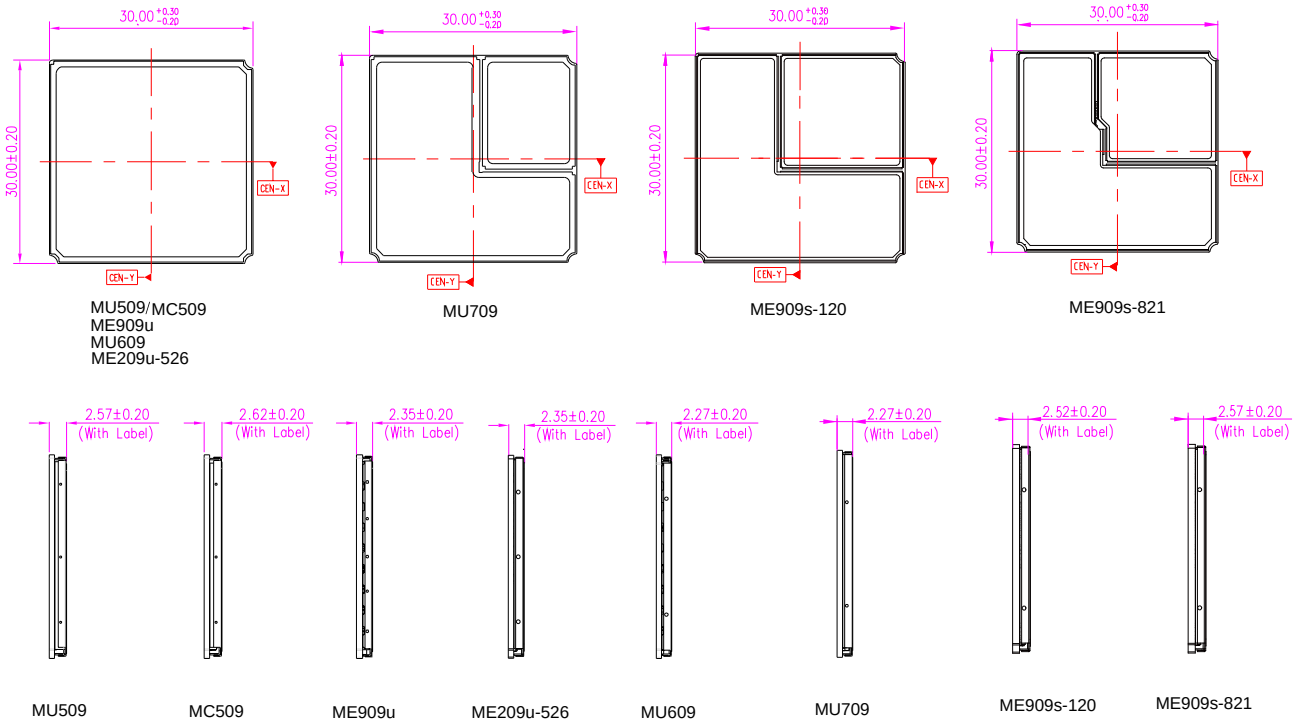
For full compatibility, please design the layout referring to MC509 size (30 mm × 30 mm × 2.65 mm ± 0.20 mm).

Table 3-1 Differences of LGA module size

LGA module	Dimension	Unit
MU509	30 × 30 × 2.6	mm
MC509	30 × 30 × 2.65	mm
MU609	30 × 30 × 2.27	mm
ME209u-526/ME909u	30 × 30 × 2.35	mm
MU709	30 × 30 × 2.27	mm
ME909s	30 × 30 × 2.52 for ME909s-120 30 × 30 × 2.57 for ME909s-821	mm

Figure 3-1 shows the dimensions of Huawei 30 mm × 30 mm LGA modules.

Figure 3-1 Dimensions of Huawei 30 mm × 30 mm LGA modules (unit: mm)

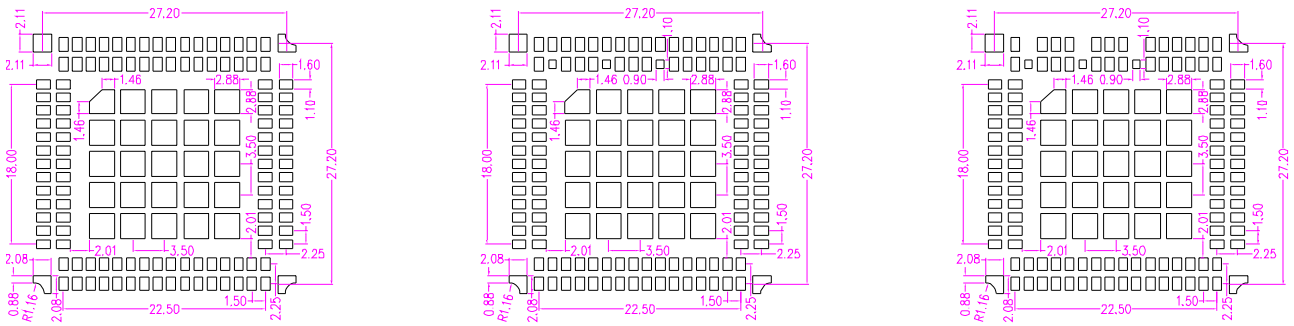


3.2 Customer PCB Design

3.2.1 PCB Pad Design

To achieve assembly yields and solder joints of high reliability, it is recommended that the PCB pad size be designed as follows:

Figure 3-2 The footprint design of Huawei 30 mm × 30 mm LGA modules (unit: mm)



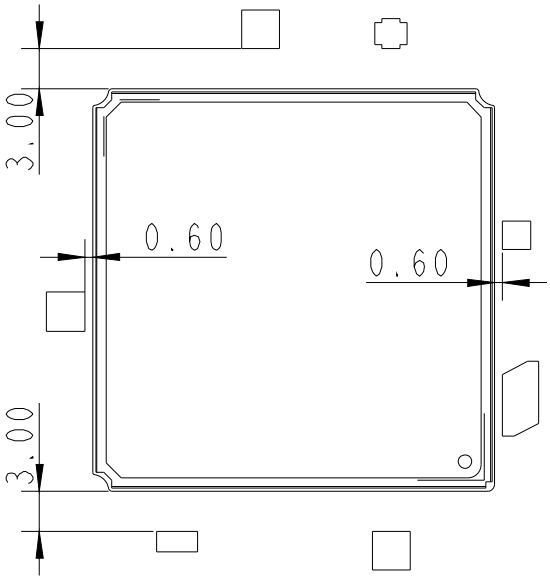
Please note that the differences of PCB pad among 30 mm × 30 mm LGA modules.

- The pin 49, pin 53 and pin 57 of MU709, ME209u-526, ME909u-523 and ME909s/MU509-65 are empty.
- The pad size and function of the antenna interface among 30 mm × 30 mm LGA modules are different, see Table 2-12 .

3.2.2 Requirements on PCB Layout

- To reduce deformation, a thickness of at least 1.0 mm is recommended.
- Other devices must be located more than 3 mm (5 mm recommended) away from the two parallel sides of the LGA module (rework requirement),and other sides with 0.6 mm. The minimum distance between the LGA module and the PCB edge is 0.3 mm.
- When the PCB layout is double sided, the module must be placed on the second side for assembly; so as to avoid module dropped from PCB or component (located in module) re-melding defects caused by uneven weight.

Figure 3-3 PCB Layout (unit: mm)



3.3 Assembly Processes

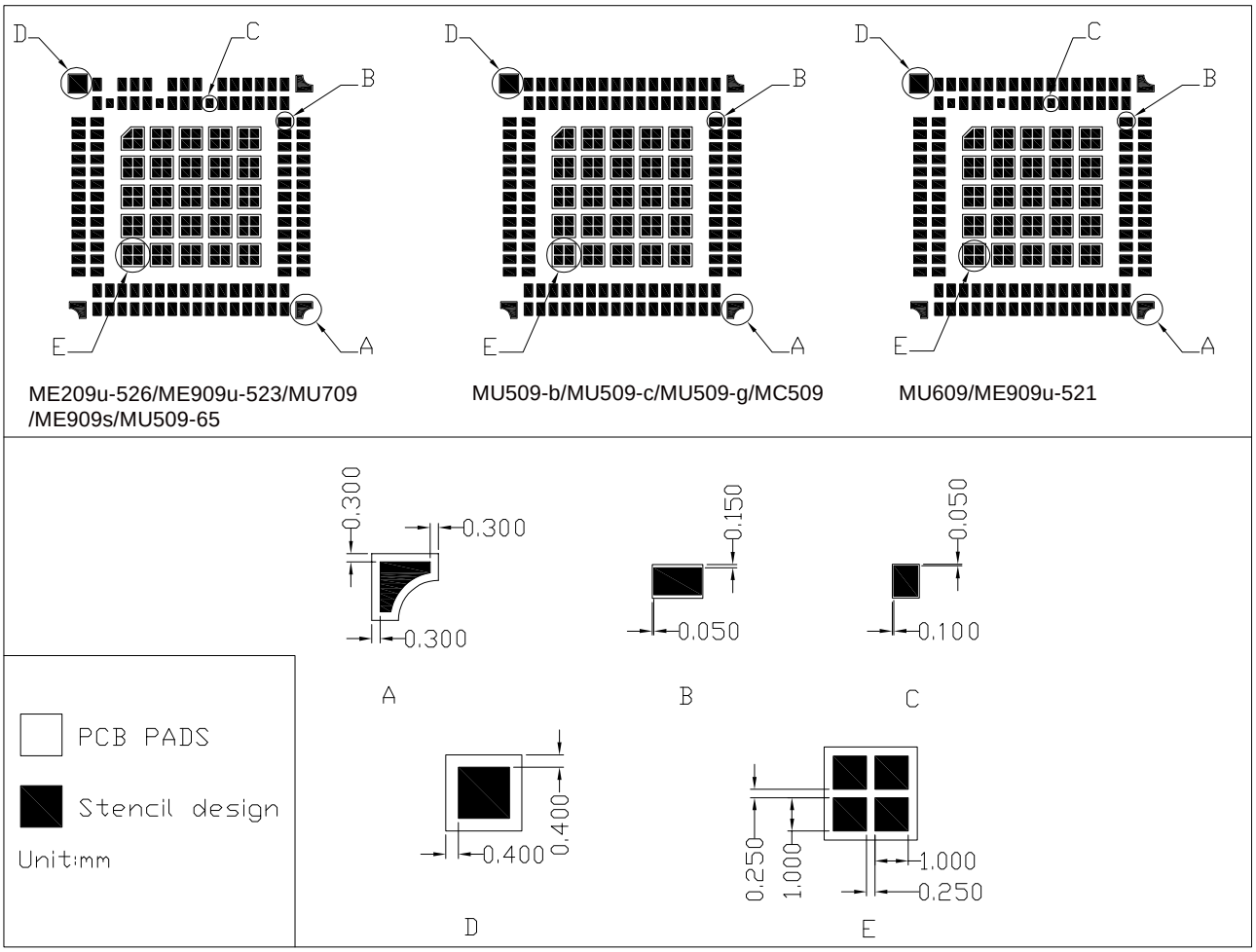
3.3.1 General Description of Assembly Processes

- Tray modules are required at SMT lines, because 30 mm × 30 mm LGA modules are placed on ESD pallets.
- Reflow ovens with at least seven temperature zones are recommended, the reflow profile please refer to Figure 3-5 .

3.3.2 Stencil Design

It is recommended that the stencil for the 30 mm × 30 mm LGA modules be 0.12 mm in thickness. For the stencil design, see Figure 3-4 .

Figure 3-4 Recommended stencil design (unit: mm)



3.3.3 Reflow Profile

For the soldering temperature of the 30 mm × 30 mm LGA modules, see the following figure.

Figure 3-5 Reflow profile

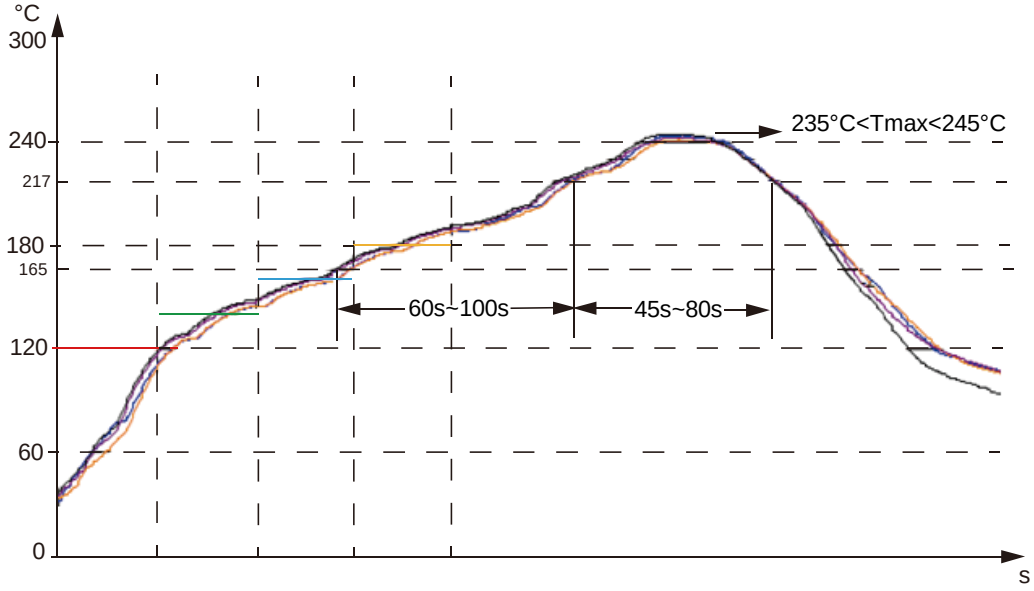


Table 3-2 Reflow parameters

Temperature Zone	Time	Key Parameter
Preheat zone (40°C–165°C)	/	Heating rate: 0.5°C/s–2°C/s
Soak zone (165°C–217°C)	(t1–t2): 60s–100s	/
Reflow zone (> 217°C)	(t3–t4): 45s–80s	Peak reflow temperature: 235°C–245°C
Cooling zone	Cooling rate: 2°C/s ≤ Slope ≤ 5°C/s	

4 Appendix

Table 4-1 Definition of LGA Interfaces

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
1	NC	-	NC	-	UART1_TX	CMOS 1.8 V	UART1_TX	CMOS 1.8 V	UART1_TX	CMOS 1.8 V	UART1_TX	CMOS 1.8 V	Reserved	-
2	NC	-	NC	-	NC	-	UART1_RTS	CMOS 1.8 V	UART1_RTS	CMOS 1.8 V	NC	-	Reserved	-
3	NC	-	NC	-	NC	-	UART1_CTS	CMOS 1.8 V	UART1_CTS	CMOS 1.8 V	NC	-	Reserved	-
4	NC	-	NC	-	UART1_RX	CMOS 1.8 V	UART1_RX	CMOS 1.8 V	UART1_RX	CMOS 1.8 V	UART1_RX	CMOS 1.8 V	Reserved	-
5	PCM_SYNC	CMOS 2.6 V	PCM_SYNC	CMOS 2.6 V	Reserved	-	PCM_SYNC	CMOS 1.8 V	PCM_SYNC[1]	CMOS 1.8 V	PCM_SYNC	CMOS 1.8 V	PCM_SYNC	CMOS 1.8 V

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
6	PCM_DIN	CMOS 2.6 V	PCM_DIN	CMOS 2.6 V	Reserved	-	PCM_DIN	CMOS 1.8 V	PCM_DIN[1]	CMOS 1.8 V	PCM_DIN	CMOS 1.8 V	PCM_DIN	CMOS 1.8 V
7	PCM_DOUT	CMOS 2.6 V	PCM_DOUT	CMOS 2.6 V	Reserved	-	PCM_DOUT	CMOS 1.8 V	PCM_DOUT[1]	CMOS 1.8 V	PCM_DOUT	CMOS 1.8 V	PCM_DOUT	CMOS 1.8 V
8	PCM_CLK	CMOS 2.6 V	PCM_CLK	CMOS 2.6 V	Reserved	-	PCM_CLK	CMOS 1.8 V	PCM_CLK[1]	CMOS 1.8 V	PCM_CLK	CMOS 1.8 V	PCM_CLK	CMOS 1.8 V
9	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_DATA1	CMOS 3.0 V	SD_DATA1	CMOS 3.0 V
10	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_DATA2	CMOS 3.0 V	SD_DATA2	CMOS 3.0 V
11	WAKEUP_IN	CMOS 2.6 V	WAKEUP_IN	CMOS 2.6 V	WAKEUP_IN	CMOS 1.8 V	WAKEUP_IN	CMOS 1.8 V	WAKEUP_IN	CMOS 1.8 V	WAKEUP_IN	CMOS 1.8 V	WAKEUP_IN	CMOS 1.8 V
12	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V
13	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V	VBAT	3.8 V
14	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V	PS_HOLD	CMOS 1.8 V	Reserved	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
15	Reserved	-	Reserved	-	SLEEP_STATUS	CMOS 1.8 V	SLEEP_STATUS	CMOS 1.8 V	SLEEP_STATUS	CMOS 1.8 V	SLEEP_STATUS	CMOS 1.8 V	SLEEP_STATUS	CMOS 1.8 V
16	NC	-	NC	-	NC	-	Reserved	-	Reserved	-	NC	-	Reserved	-
17	NC	-	NC	-	NC	-	Reserved	-	Reserved	-	NC	-	Reserved	-
18	NC	-	NC	-	NC	-	Reserved	-	Reserved	-	NC	-	Reserved	-
19	NC	-	NC	-	NC	-	Reserved	-	Reserved	-	NC	-	Reserved	-
20	NC	-	NC	-	NC	-	Reserved	-	Reserved	-	NC	-	Reserved	-
21	NC	-	NC	-	NC	-	ANT_TUNE0[1]	CMOS 1.8 V	ANT_TUNE0[1]	CMOS 1.8 V	NC	-	Reserved	-
22	NC	-	NC	-	NC	-	ANT_TUNE1[1]	CMOS 1.8 V	ANT_TUNE1[1]	CMOS 1.8 V	NC	-	Reserved	-
23	NC	-	NC	-	NC	-	ANT_TUNE2[1]	CMOS 1.8 V	ANT_TUNE2[1]	CMOS 1.8 V	NC	-	Reserved	-
24	NC	-	NC	-	NC	-	ANT_TUNE3[1]	CMOS 1.8 V	ANT_TUNE3[1]	CMOS 1.8 V	NC	-	Reserved	-
25	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
26	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
27	NC	-	NC	-	NC	-	Reserved	-	Reserved	-	NC	-	Reserved	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
28	Reserved	-	Reserved	-	Reserved	-	UART2_TX	CMOS 1.8 V	UART2_TX	CMOS 1.8 V	Reserved	-	UART2_TX	CMOS 1.8 V
29	Reserved	-	Reserved	-	Reserved	-	UART2_RX	CMOS 1.8 V	UART2_RX	CMOS 1.8 V	Reserved	-	UART2_RX	CMOS 1.8 V
30	JTAG_TMS	CMOS 1.8 V	JTAG_TMS	CMOS 2.6 V	JTAG_TMS	CMOS 1.8 V	JTAG_TMS	CMOS 1.8 V	JTAG_TMS	CMOS 1.8 V	JTAG_TMS	CMOS 1.8 V	JTAG_TMS	CMOS 1.8 V
31	VCC_EXT2	2.6 V	VCC_EXT2	2.6 V	NC	-	NC	-	NC	-	Reserved	-	Reserved	-
32	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V	VCC_EXT1	1.8 V
33	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	Reserved	-
34	USIM _VCC	1.8 V/2.85 V	RUIM_VCC	1.8 V/2.85 V	USIM_VCC	1.8 V/2.85 V	USIM_VCC	1.8 V/2.85 V	USIM_VCC	1.8 V/2.85 V	USIM_VCC	1.8 V/3.0 V	USIM_VCC	1.8 V/3.0 V
35	VCOIN	-	VCOIN	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
36	JTAG_TRST_N	CMOS 1.8 V	JTAG_TRST_N	CMOS 2.6 V	JTAG_TRST_N	CMOS 1.8 V	JTAG_TRST_N	CMOS 1.8 V	JTAG_TRST_N	CMOS 1.8 V	JTAG_TRST_N	CMOS 1.8 V	JTAG_TRST_N	CMOS 1.8 V
37	NC	--	NC	--	NC	-	NC	-	NC	-	NC	-	Reserved	-
38	MIC2_P	-	MIC2_P	-	NC	-	NC	-	NC	-	NC	-	NC	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
39	MIC2_N	-	MIC2_N	-	NC	-	NC	-	NC	-	NC	-	NC	-
40	MIC1_P	-	MIC1_P	-	NC	-	NC	-	NC	-	NC	-	NC	-
41	MIC1_N	-	MIC1_N	-	NC	-	NC	-	NC	-	NC	-	NC	-
42	JTAG_TCK	CMOS 1.8 V	JTAG_TCK	CMOS 2.6 V	JTAG_TCK	CMOS 1.8 V	JTAG_TCK	CMOS 1.8 V	JTAG_TCK	CMOS 1.8 V	JTAG_TCK	CMOS 1.8 V	JTAG_TCK	CMOS 1.8 V
43	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	GPIO	-
44	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
45	GPIO	CMOS 2.6 V	W_DISABLE	CMOS 2.6 V	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
46	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	Reserved	-	Reserved	-	Reserved	-	Reserved	-	GPIO	-
47	NC	-	NC	-	NC	-	JTAG_SRST_N	CMOS 1.8 V	JTAG_SRST_N	CMOS 1.8 V	NC	-	NC	-
48	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
49	GND NOT USED is only for MU509-65	-	GND	-	GND	-	GND	-	NOT USED	-	NOT USED	-	NOT USED	-
50	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
51	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO2	CMOS 1.8 V
52	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
53	GND NOT USED is only for MU509-65	-	GND	-	GND	-	GND	-	NOT USED	-	NOT USED	-	NOT USED	-
54	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
55	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO5/USIM_Switch	CMOS 1.8 V
56	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
57	GND NOT USED is only for MU509-65	-	GND	-	GND	-	GND	-	NOT USED	-	NOT USED	-	NOT USED	-
58	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
59	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
60	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
61	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
62	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
63	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
64	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
65	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
66	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_DATA3	CMOS 3.0 V	SD_DATA3	CMOS 3.0 V
67	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_CLK	CMOS 3.0 V	SD_CLK	CMOS 3.0 V
68	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_DATA0	CMOS 3.0 V	SD_DATA0	CMOS 3.0 V
69	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_CMD	CMOS 3.0 V	SD_CMD	CMOS 3.0 V
70	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-	USIM_DET	CMOS 1.8 V
71	WAKEUP_OUT	CMOS 2.6 V	WAKEUP_OUT	CMOS 2.6 V	WAKEUP_OUT	CMOS 1.8 V	WAKEUP_OUT	CMOS 1.8 V	WAKEUP_OUT	CMOS 1.8 V	WAKEUP_OUT	CMOS 1.8 V	WAKEUP_OUT	CMOS 1.8 V
72	JTAG_TDO	CMOS 1.8 V	JTAG_TDO	CMOS 2.6 V	JTAG_TDO	CMOS 1.8 V	JTAG_TDO	CMOS 1.8 V	JTAG_TDO	CMOS 1.8 V	JTAG_TDO	CMOS 1.8 V	JTAG_TDO	CMOS 1.8 V

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
73	UART0_DSR	CMOS 2.6 V	UART0_DSR	CMOS 2.6 V	UART0_DSR	CMOS 1.8 V	Reserved	-	Reserved	-	UART0_DSR	CMOS 1.8 V	UART0_DSR	CMOS 1.8 V
74	UART0_RTS	CMOS 2.6 V	UART0_RTS	CMOS 2.6 V	UART0_RTS	CMOS 1.8 V	UART0_RTS	CMOS 1.8 V	UART0_RTS	CMOS 1.8 V	UART0_RTS	CMOS 1.8 V	UART0_RTS	CMOS 1.8 V
75	UART0_DCD	CMOS 2.6 V	UART0_DCD	CMOS 2.6 V	UART0_DCD	CMOS 1.8 V	Reserved	-	Reserved	-	UART0_DCD	CMOS 1.8 V	UART0_DCD	CMOS 1.8 V
76	UART0_TX	CMOS 2.6 V	UART0_TX	CMOS 2.6 V	UART0_TX	CMOS 1.8 V	UART0_TX	CMOS 1.8 V	UART0_TX	CMOS 1.8 V	UART0_TX	CMOS 1.8 V	UART0_TX	CMOS 1.8 V
77	UART0_RING	CMOS 2.6 V	UART0_RING	CMOS 2.6 V	UART0_RING	CMOS 1.8 V	Reserved	-	Reserved	-	UART0_RING	CMOS 1.8 V	UART0_RING	CMOS 1.8 V
78	UART0_RX	CMOS 2.6 V	UART0_RX	CMOS 2.6 V	UART0_RX	CMOS 1.8 V	UART0_RX	CMOS 1.8 V	UART0_RX	CMOS 1.8 V	UART0_RX	CMOS 1.8 V	UART0_RX	CMOS 1.8 V
79	UART0_DTR	CMOS 2.6 V	UART0_DTR	CMOS 2.6 V	UART0_DTR	CMOS 1.8 V	Reserved	-	Reserved	-	UART0_DTR	CMOS 1.8 V	UART0_DTR	CMOS 1.8 V
80	UART0_CTS	CMOS 2.6 V	UART0_CTS	CMOS 2.6 V	UART0_CTS	CMOS 1.8 V	UART0_CTS	CMOS 1.8 V	UART0_CTS	CMOS 1.8 V	UART0_CTS	CMOS 1.8 V	UART0_CTS	CMOS 1.8 V

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
81	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	Pulled up on module	POWER_ON_OFF	CMOS 1.8 V
82	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
83	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
84	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
85	USB_DM		USB_DM		USB_DM	-	USB_DM	-	USB_DM	-	USB_DM	-	USB_DM	-
86	USB_DP		USB_DP		USB_DP	-	USB_DP	-	USB_DP	-	USB_DP	-	USB_DP	-
87	JTAG_TDI	CMOS 1.8 V	JTAG_TDI	CMOS 2.6 V	JTAG_TDI	CMOS 1.8 V	JTAG_TDI	CMOS 1.8 V	JTAG_TDI	CMOS 1.8 V	JTAG_TDI	CMOS 1.8 V	JTAG_TDI	CMOS 1.8 V
88	USIM_RESET	1.8 V /2.85 V	RUIM_RESET	1.8 V /2.85 V	USIM_RESET	1.8 V /2.85 V	USIM_RESET	1.8 V /2.85 V	USIM_RESET	1.8 V /2.85 V	USIM_RESET	1.8 V /3.0 V	USIM_RESET	1.8 V /3.0 V
89	USIM_DATA	1.8 V/2.85 V	RUIM_DATA	1.8 V /2.85 V	USIM_DATA	1.8 V /2.85 V	USIM_DATA	1.8 V /2.85 V	USIM_DATA	1.8 V /2.85 V	USIM_DATA	1.8 V /3.0 V	USIM_DATA	1.8 V /3.0 V
90	USIM_CLK	1.8 V /2.85 V	RUIM_CLK	1.8 V /2.85 V	USIM_CLK	1.8 V /2.85 V	USIM_CLK	1.8 V /2.85 V	USIM_CLK	1.8 V /2.85 V	USIM_CLK	1.8 V /3.0 V	USIM_CLK	1.8 V /3.0 V

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
91	LED_STATUS	SINK	LED_STATUS	SINK	Reserved	-	Reserved	-	Reserved	-	Reserved	-	Reserved	-
92	NC	-	NC	-	Reserved	-	Reserved	-	Reserved	-	SD_VCC	3.0 V	SD_VCC	-
93	JTAG_RTCK	CMOS 1.8 V	JTAG_RTCK	CMOS 2.6 V	JTAG_RTCK	CMOS 1.8 V	JTAG_RTCK	CMOS 1.8 V	JTAG_RTCK	CMOS 1.8 V	NC	-	JTAG_RTCK	CMOS 1.8 V
94	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	Reserved	-
95	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	Reserved	-
96	EAR_OUT_N	-	EAR_OUT_N	-	NC	-	NC	-	NC	-	NC	-	Reserved	-
97	EAR_OUT_P	-	EAR_OUT_P	-	NC	-	NC	-	NC	-	NC	-	Reserved	-
98	SPKR_OUT_P	-	SPKR_OUT_P	-	NC	-	NC	-	NC	-	NC	-	Reserved	-
99	SPKR_OUT_N	-	SPKR_OUT_N	-	NC	-	NC	-	NC	-	NC	-	Reserved	-
100	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V	RESIN_N	CMOS 1.8 V
101	LED_MODE	SINK	LED_MODE	SINK	LED_MODE	SINK	LED_MODE[1]	SINK	LED_MODE[1]	SINK	LED_MODE	SINK	LED_MODE	SINK
102	NC	-	NC	-	Reserved	-	Reserved	-	ADC_1	-	Reserved	-	ADC_1	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
103	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	Reserved	-
104	NC	-	NC	-	NC	-	Reserved		ADC_2	-	Reserved	-	ADC_2	-
105	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO1	CMOS 1.8 V
106	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
107	MAIN_ANT	-	MAIN_ANT	-	MAIN_ANT	-	MAIN_ANT	-	MAIN_ANT	-	MAIN_ANT	-	MAIN_ANT	-
108	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
109	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO4	CMOS 1.8 V
110	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
111	NC	-	GPS_ANT	-	GPS_ANT	-	GPS_ANT	-	GPS_ANT (for ME909u-523) NC (for ME209u-526)	-	NC	-	NC	-
112	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
113	GPIO	CMOS 2.6 V	GPIO	CMOS 2.6 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO	CMOS 1.8 V	GPIO3	CMOS 1.8 V
114	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
115	NC	-	AUX_ANT	-	AUX_ANT	-	AUX_ANT	-	AUX_ANT	-	AUX_ANT	-	AUX_ANT	-
116	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
117	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
118	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
119	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
120	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-	NC	-
121	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
122	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
123	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
124	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
125	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
126	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
127	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
128	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
129	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
130	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
131	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
132	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-

Pin No.	MU509		MC509		MU609		ME909u-521		ME909u-523/ME209u-526		MU709		ME909s	
	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level	Signal Definition	Level
133	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
134	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
135	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
136	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
137	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
138	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
139	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
140	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
141	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
142	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
143	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
144	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-
145	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-	GND	-

NOTE

- The NC pins are not connected, therefore, before you deal with these pins, please refer to the corresponding hardware guide.
- The Reserved pins are internally connected to the modules. Therefore, these pins should not be used, otherwise they may cause problems. Please contact with us for more details about this information.
- [1] The firmware does not support these features yet.

Figure 4-2 Top view of sequence of MU509-b/MU509-c/MU509-g and MC509 interface pins

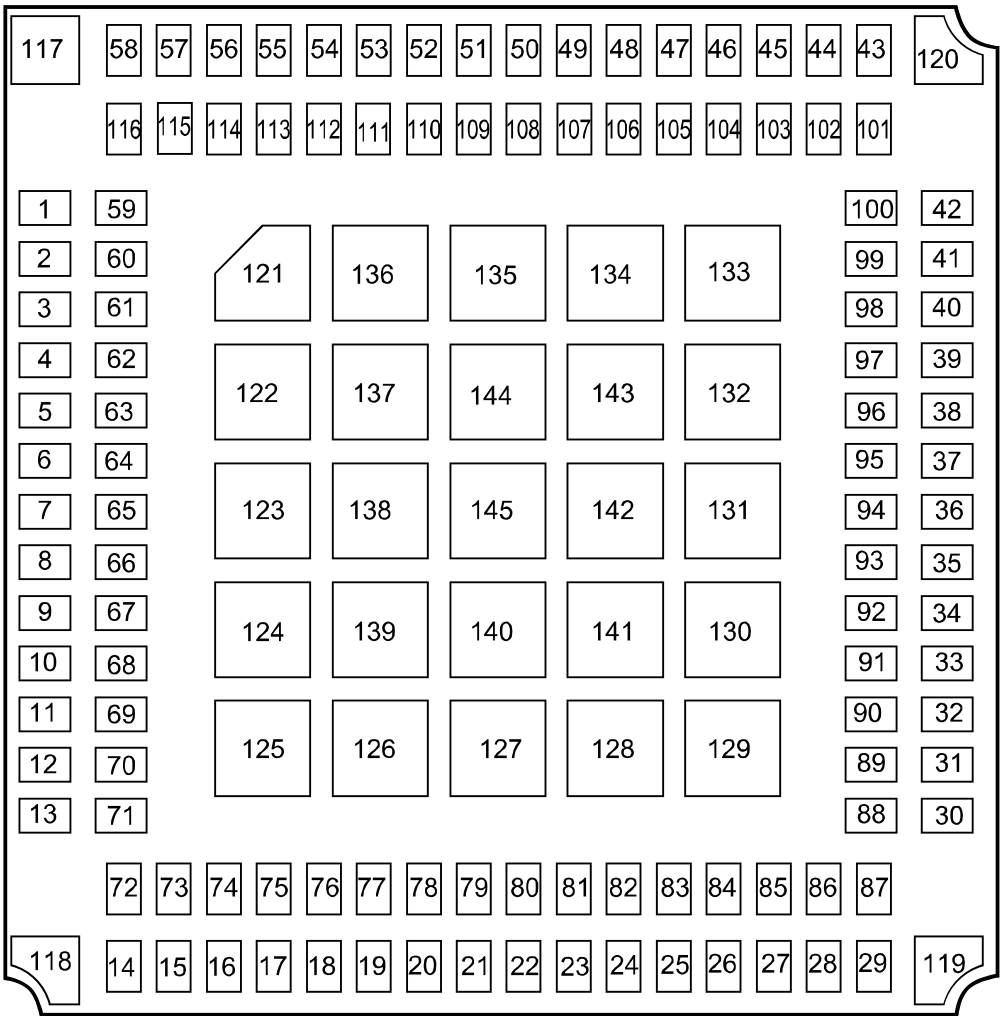


Figure 4-3 Top view of sequence of MU609/ME909u-521 interface pins

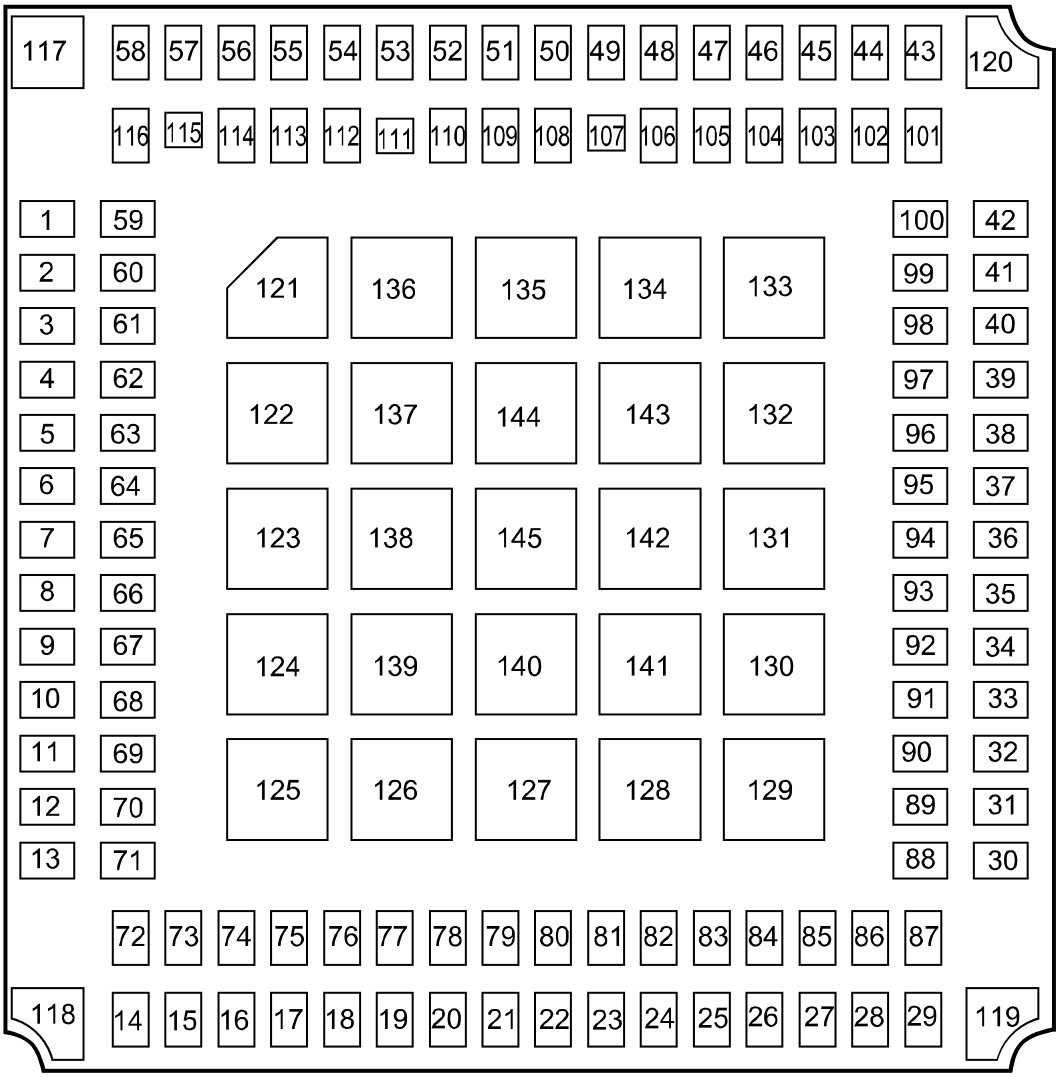
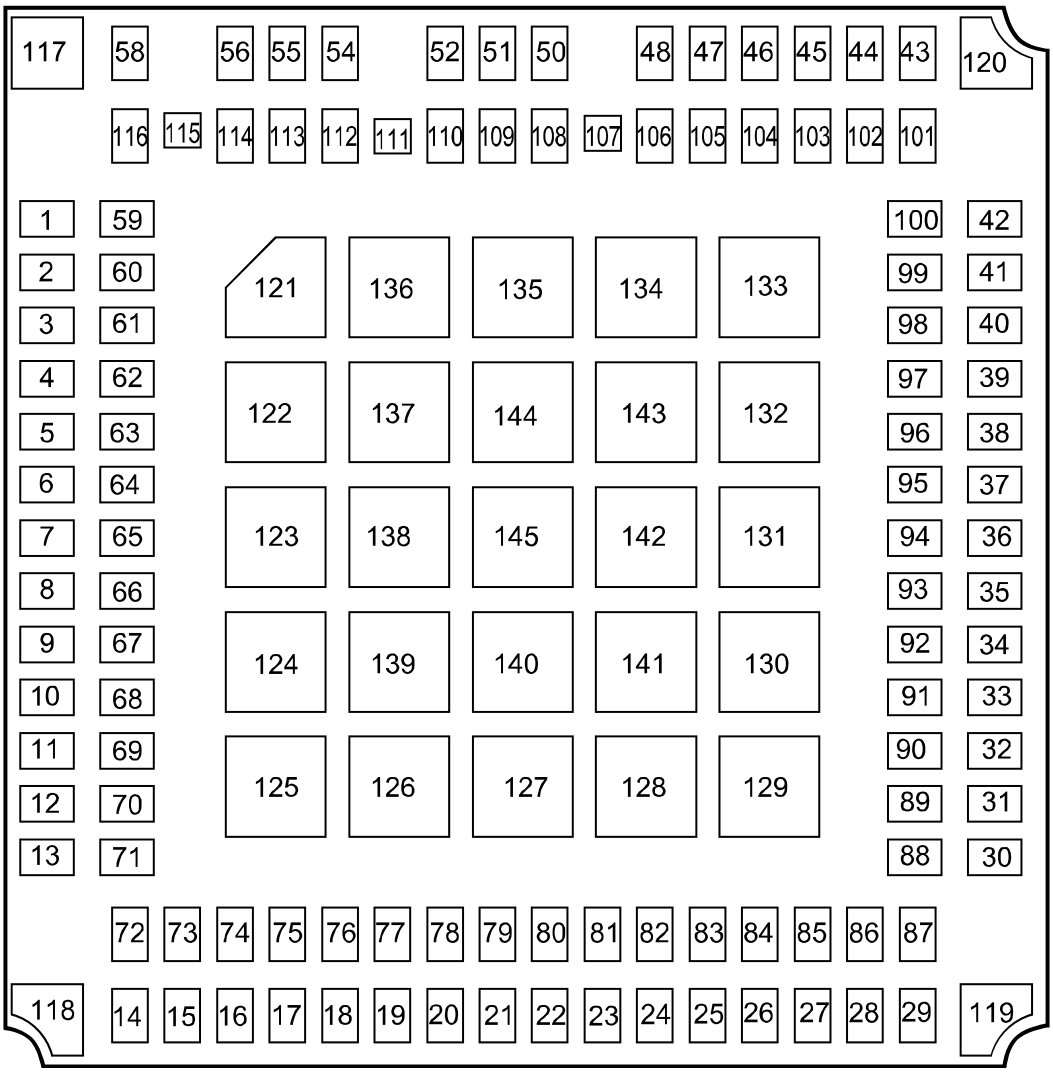


Figure 4-4 Top view of sequence of MU709/ME209u-526/ME909u-523/ME909s/MU509-65 interface pins



5 Acronyms and Abbreviations

Acronym or Abbreviation	Expansion
AUX	Auxiliary
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
DC	Direct Current
DCE	Data Communication Equipment
DL	Down Link
DTE	Data Terminal Equipment
EDGE	Enhanced Data Rate for GSM Evolution
ESD	Electrostatic Discharge
EV-DOrA	Evolution Data Only Release A
GPIO	General-purpose I/O
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HSDPA	High-Speed Downlink Packet Access
HSPA	Enhanced High Speed Packet Access
HSUPA	High Speed Up-link Packet Access
IC	Integrated Circuit
JTAG	Joint Test Action Group
LED	Light-Emitting Diode
LGA	Land Grid Array

Acronym or Abbreviation	Expansion
LTE	Long Term Evolution
NC	Not Connected
PA	Power Amplifier
PCB	Printed Circuit Board
RF	Radio Frequency
RUIM	Removable User Identity Module
SMS	Short Message Service
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver-Transmitter
UL	Up Link
UIM	User Identity Module
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
WCDMA	Wideband Code Division Multiple Access